datasheet

PRELIMINARY SPECIFICATION

1/3.8" color CMOS (1392 x 976) high dynamic range (HDR)
high definition (HD) image sensor

OV9716

color CMOS (1392x976) high dynamic range (HDR) high definition image sensor

datasheet (a-BGA™)
PRELIMINARY SPECIFICATION

version 1.22
march 2019

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applications

- automotive
  - 360° surround view system
  - rear view camera
  - lane departure warning/ lane keep assist
  - blind spot detection
  - pedestrian detection
  - traffic sign recognition
  - occupant sensor
  - camera monitoring system/ e-mirror
  - autonomous driving

ordering information

- **OV09716-B77Y-1E-Z** (color, lead-free) 77-pin a-BGA™, with DAR coating, rev 1E, packed in tray
- **OV09716-B77Y-LE-Z** (color, lead-free) 77-pin a-BGA™, with DAR coating, rev 1E, packed in tray with protective film (tab top left)
- **OV09716-B77Y-OE-Z** (color, lead-free) 77-pin a-BGA™, with DAR coating, rev 1E, packed in tape & reel with protective film (tab top left)

note Since it is impossible to check compatibility with all displays, check interoperability before committing to mass production.

features

- support for image size: 1392x976, VGA, QVGA, and any cropped size
- high dynamic range
- high sensitivity
- low power consumption
- image sensor processor functions: lens correction, defective pixel cancelation, HDR combination, and automatic black level correction
- supported output formats: RAW
- horizontal and vertical sub-sampling
- SCCB for register programming
- high speed serial data transfer with MIPI CSI-2
- parallel 12-bit DVP output
- external frame synchronization capability
- embedded temperature sensor
- one time programmable (OTP) memory

note To reduce image artifacts from infrared light and provide the best image quality, OmniVision recommends an IR-cut filter

key specifications (typical)

- **active array size:** 1392 x 976
- **power supply:**
  SVDD, SVDD_pix, PVDD (analog): 3.14 ~ 3.47V
  DVDD (digital): 1.14 ~ 1.3V
  DOVDD (digital): 1.7 ~ 1.9V
  AVDD18 (analog): 1.7 ~ 1.9V
- **power consumption (typical):**
  active: TBD
  standby: TBD
- **temperature range:**
  operating: -40°C to 105°C sensor ambient temperature and -40°C to 132°C junction temperature (see **table 8-2**)
- **output interfaces:** up to 4-lane MIPI CSI-2, 12-bit DVP
- **input clock frequency:** 6 ~ 36 MHz
- **lens size:** 1/3.8"
- **lens chief ray angle:** 15° (see **figure 10-2**)
- **output formats:** single exposure HDR - 16-bit combined RAW, 12-bit compressed combined RAW; dual exposure HDR - 16-bit combined RAW + 12-bit VS RAW, 12-bit compressed combined RAW + 12-bit VS RAW, 3x12 bit RAW, 3x10 bit RAW
- **scan mode:** progressive
- **shutter:** rolling shutter
- **maximum image transfer rate:** 60 fps full resolution
- **sensitivity:** 27,500 e^-/Lux-sec
- **max S/N ratio:** 41 dB
- **dynamic range:** 120 dB
- **pixel size:** 2.8 µm x 2.8 µm
- **image area:** 3942.4 µm x 2777.6 µm
- **package dimensions:** 8 mm x 8 mm

note Pixel performance and power requirements are estimates. Values may change based on real measurements.

note The OV9716 will be qualified to AEC-Q100 grade-2 specifications.

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1 application system

1.1 overview

The OV9716 color image sensor is a 1/3.8" optical format, 1392x976 single-chip, low power CMOS, active-pixel, digital high dynamic range sensor for mainstream automotive market.

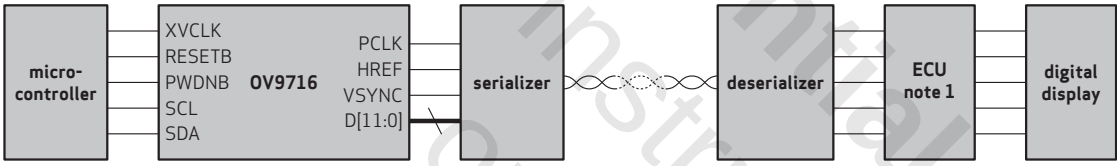
The OV9716 features OmniBSI-2™ technology to extend the dynamic range. The OV9716 has the option to output a 16-bit, 60 fps video stream with 84 dB dynamic range from a single exposure. The sensor supports dual exposure staggered HDR for 120 dB. In this case, the HDR combination is done externally from the 16-bit first plus 12-bit second exposure output.

The OV9716 performs sophisticated camera functions on-chip controlled via the SCCB interface. These functions include lens shading correction, dual conversion gain (DCG) combination, and defect pixel correction. The OV9716 enables advanced HDR imaging in a simple, cost effective system.

1.1.1 typical OV9716 standalone camera

figure 1-1 shows the block diagram of a standalone OV9716 camera for automotive applications. The microcontroller programs the register settings and controls the OV9716 based on the application requirements. The serializer and deserializer (SerDes) pair is for transferring video from the camera to the display unit over a long distance.

figure 1-1 standalone camera block diagram for automotive applications

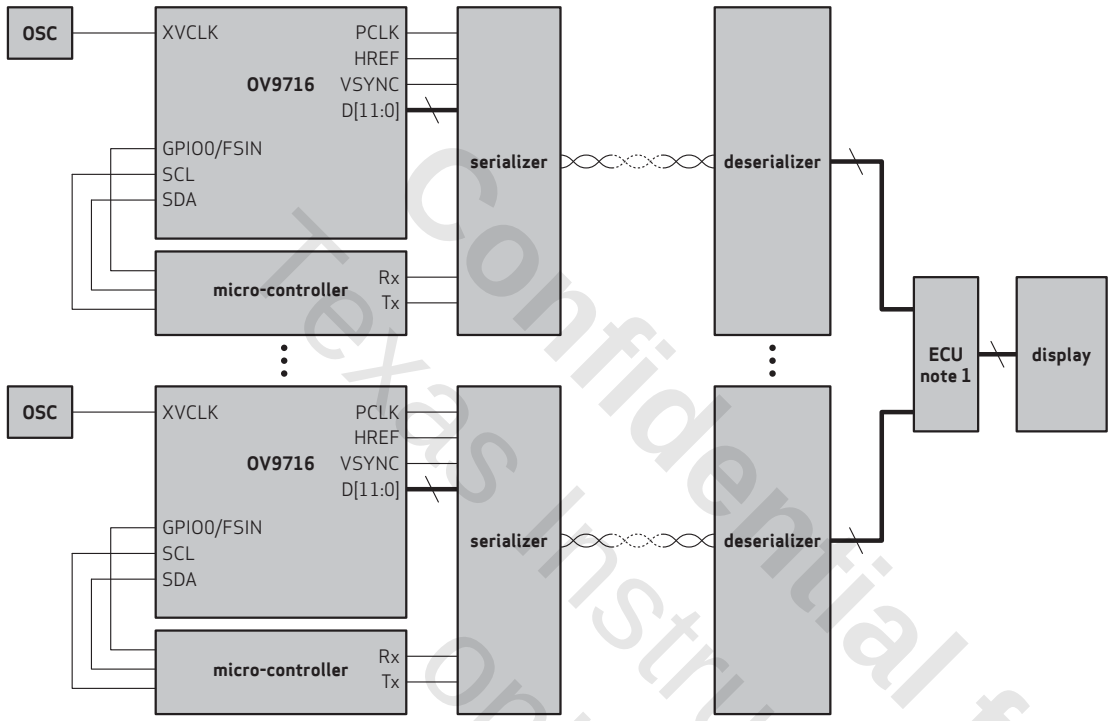


note 1 OV491 or similar ISP processor is required to generate YUV or RGB for digital display

1.1.2 typical OV9716 multi-camera system

The OV9716 features frame sync input to synchronize the video streaming timing between multiple sensors in a multi-camera system. **figure 1-2** shows the block diagram of a typical multi-camera system using the OV9716. The sensor registers are programmed by the electronic control unit (ECU) microcontroller from the back channel.

figure 1-2 multi-camera block diagram



note 1 OV491 or similar ISP processor is required to generate YUV or RGB for digital display

1.2 signal description and pin assignment

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV9716 image sensor. The package information is shown in **section 9**.

figure 1-3 pin diagram

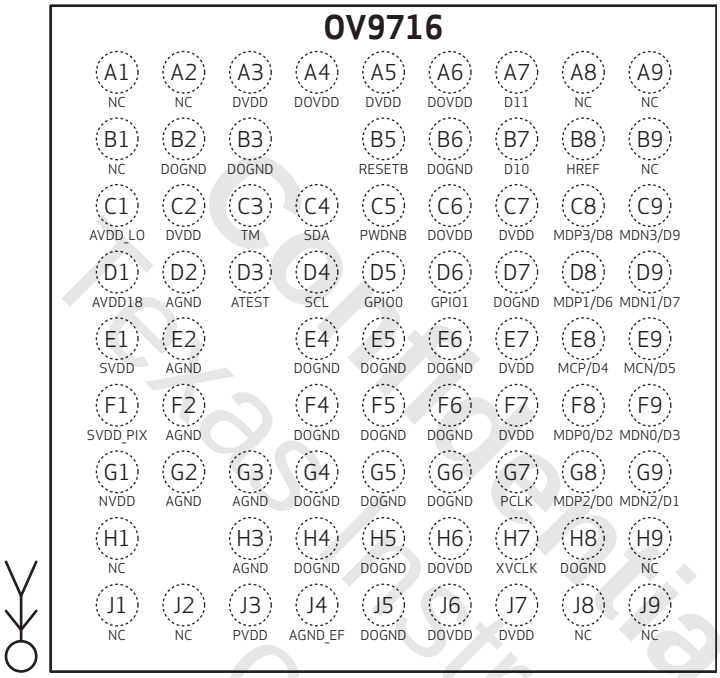


table 1-1 signal descriptions (sheet 1 of 4)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	NC	–	no connect
A3	DVDD	power	digital circuit power
A4	DOVDD	power	I/O power
A5	DVDD	power	digital circuit power
A6	DOVDD	power	I/O power
A7	**D11**	output	DVP data output
A8	NC	–	no connect
A9	NC	–	no connect

table 1-1 signal descriptions (sheet 2 of 4)

pin number	signal name	pin type	description
B1	NC	–	no connect
B2	DOGND	ground	ground for I/O and digital circuit
B3	DOGND	ground	ground for I/O and digital circuit
B5	**RESETB**	input	reset/power down (active low with pull up resistor)
B6	DOGND	ground	ground for I/O and digital circuit
B7	**D10**	output	DVP data output
B8	**HREF**	output	video output horizontal signal
B9	NC	–	no connect
C1	AVDD_LO	analog I/O	AVDD_LO regulated supply
C2	DVDD	power	digital circuit power
C3	**TM**	input	test mode (active high with pull down resistor)
C4	**SDA**	I/O	SCCB interface data pin
C5	**PWDNB**	input	power down (active low with pull up resistor)
C6	DOVDD	power	I/O power
C7	DVDD	power	digital circuit power
C8	**MDP3/D8**	output	MIPI data output/DVP data output
C9	**MDN3/D9**	output	MIPI data output/DVP data output
D1	AVDD18	power	analog power
D2	AGND	ground	analog ground
D3	ATEST	analog I/O	analog test I/O
D4	**SCL**	input	SCCB interface input clock
D5	**GPIO0**	I/O	general purpose I/O
D6	**GPIO1**	I/O	general purpose I/O
D7	DOGND	ground	ground for I/O and digital circuit
D8	**MDP1/D6**	output	MIPI data output/DVP data output
D9	**MDN1/D7**	output	MIPI data output/DVP data output
E1	SVDD	SVDD	power
E2	AGND	ground	analog ground
E4	DOGND	ground	ground for I/O and digital circuit
E5	DOGND	ground	ground for I/O and digital circuit

table 1-1 signal descriptions (sheet 3 of 4)

pin number	signal name	pin type	description
E6	DOGND	ground	ground for I/O and digital circuit
E7	DVDD	power	digital circuit power
E8	**MCP/D4**	output	MIPI clock output/DVP data output
E9	**MCN/D5**	output	MIPI clock output/DVP data output
F1	SVDD_PIX	power	sensor power (pixel array)
F2	AGND	ground	analog ground
F4	DOGND	ground	ground for I/O and digital circuit
F5	DOGND	ground	ground for I/O and digital circuit
F6	DOGND	ground	ground for I/O and digital circuit
F7	DVDD	power	digital circuit power
F8	**MDP0/D2**	output	MIPI data output/DVP data output
F9	**MDN0/D3**	output	MIPI data output/DVP data output
G1	NVDD	analog I/O	NVDD regulated supply
G2	AGND	ground	analog ground
G3	AGND	ground	analog ground
G4	DOGND	ground	ground for I/O and digital circuit
G5	DOGND	ground	ground for I/O and digital circuit
G6	DOGND	ground	ground for I/O and digital circuit
G7	**PCLK**	I/O	DVP clock input
G8	**MDP2/D0**	output	MIPI data output/DVP data output
G9	**MDN2/D1**	output	MIPI data output/DVP data output
H1	NC	–	no connect
H3	AGND	ground	analog ground
H4	DOGND	ground	ground for I/O and digital circuit
H5	DOGND	ground	ground for I/O and digital circuit
H6	DOVDD	power	I/O power
H7	**XVCLK**	input	clock input
H8	DOGND	ground	ground for I/O and digital circuit
H9	NC	–	no connect
J1	NC	–	no connect

table 1-1 signal descriptions (sheet 4 of 4)

pin number	signal name	pin type	description
J2	NC	–	no connect
J3	PVDD	power	PLL power supply
J4	AGND_EF	ground	analog ground
J5	DOGND	ground	ground for I/O and digital circuit
J6	DOVDD	power	I/O power
J7	DVDD	power	digital circuit power
J8	NC	–	no connect
J9	NC	–	no connect

table 1-2 pin states under various conditions (sheet 1 of 2)

pin number	signal name	RESETB = 0	RESETB = 1, PWDNB = 1 stream/standby	RESETB = 1, PWDNB = 0 hardware standby/power down
A7	D11	output[a]	output (configurable)[b]	output (configurable)[b]
B5	RESETB	input	input	input
B7	D10	output[a]	output (configurable)[b]	output (configurable)[b]
B8	HREF	output[a]	output (configurable)[b]	output (configurable)[b]
C3	TM	input	input	input
C4	SDA	open-drain	open-drain	open-drain
C5	PWDNB	input	input	input
C8	MDP3/D8	output[a]	output (configurable)[b]	output (configurable)[b]
C9	MDN3/D9	output[a]	output (configurable)[b]	output (configurable)[b]
D4	SCL	input	input	input
D5	GPIO0	input	input (configurable)	input (configurable)
D6	GPIO1	input	input (configurable)	input (configurable)
D8	MDP1/D6	output[a]	output (configurable)[b]	output (configurable)[b]
D9	MDN1/D7	output[a]	output (configurable)[b]	output (configurable)[b]
E8	MCP/D4	output[a]	output (configurable)[b]	output (configurable)[b]
E9	MCN/D5	output[a]	output (configurable)[b]	output (configurable)[b]
F8	MDP0/D2	output[a]	output (configurable)[b]	output (configurable)[b]

table 1-2 pin states under various conditions (sheet 2 of 2)

pin number	signal name	RESETB = 0	RESETB = 1, PWDNB = 1 stream/standby	RESETB = 1, PWDNB = 0 hardware standby/power down
F9	MDN0/D3	output[a]	output (configurable)[b]	output (configurable)[b]
G7	PCLK	output[a]	output (configurable)[b]	output (configurable)[b]
G8	MDP2/D0	output[a]	output (configurable)[b]	output (configurable)[b]
G9	MDN2/D1	output[a]	output (configurable)[b]	output (configurable)[b]
H7	XVCLK	input	input	input

a. tri-stated

b. 0x3488[5]: drive-value, 0x3488[4]: drive enable

table 1-3 pad equivalent circuit (sheet 1 of 2)

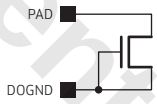
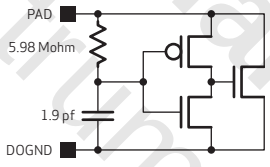
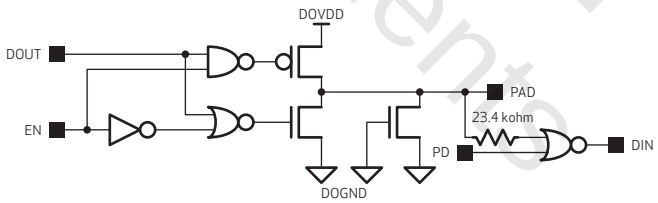
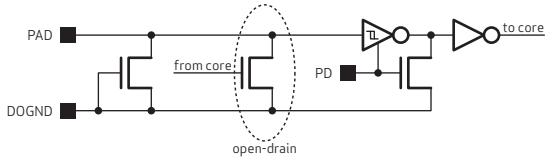
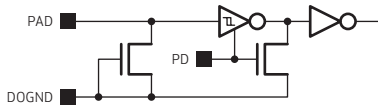
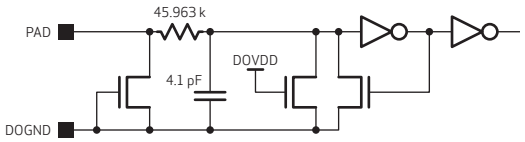
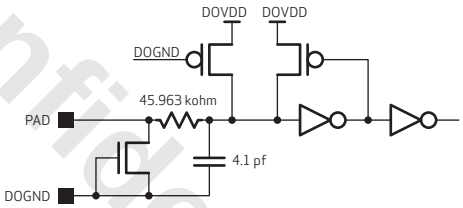
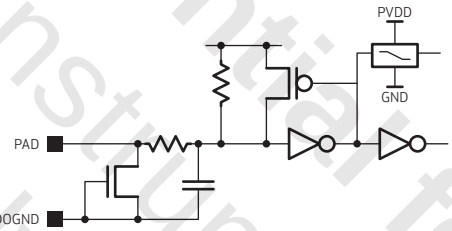
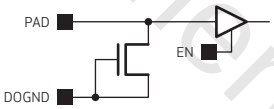
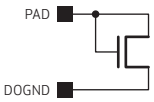
signal name	equivalent circuit
DOGND, DOVDD, ATEST, SVDD_PIX, AGND	
DVDD, SVDD, PVDD, AVDD18	
GPIO0, GPIO1, HREF, D10, D11, MDN3/D9, MDP3/D8, MDN1/D7, MDP1/D6, MCN/D5, MCP/D4, MDN0/D3, MDP0/D2, MDN2/D1, MDP2/D0, PCLK	
SDA	

table 1-3 pad equivalent circuit (sheet 2 of 2)

signal name	equivalent circuit
SCL	
TM	
RESETB	
PWDNB	
XVCLK	
NVDD	

1.3 reference design

figure 1-4 shows the power supply and signal connection of the OV9716 when using MIPI interface. The SCCB ID is defined by the voltage level of GPIO1 at power up and after hardware reset (RESETB pin low). When it is pulled down, the SCCB ID is "6C" by default, or defined by 0x300C. When it is pulled high, the SCCB ID is 0x20.

The pixel array is powered from 3.3V (SVDD). Analog supply is 1.8V (AVDD18) and 3.3V (SVDD_PIX). I/O pad power (DOVDD) is 1.8V. Core logic operates on 1.2V (DVDD). The OV9716 must use external power de-coupling capacitors to reduce noise. The recommended capacitance is 1µF. At power up, the power supplies should ramp up in 50 µs or more to avoid in-rush current during ramp-up.

figure 1-4 OV9716 MIPI reference schematic

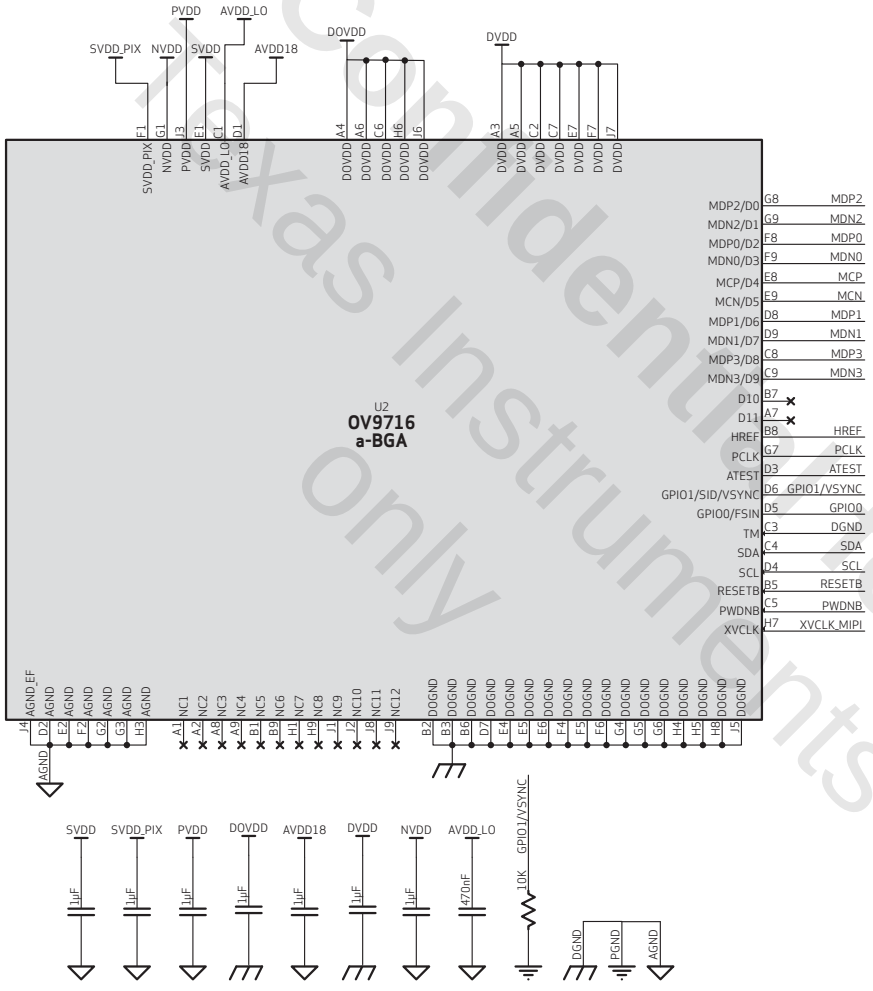
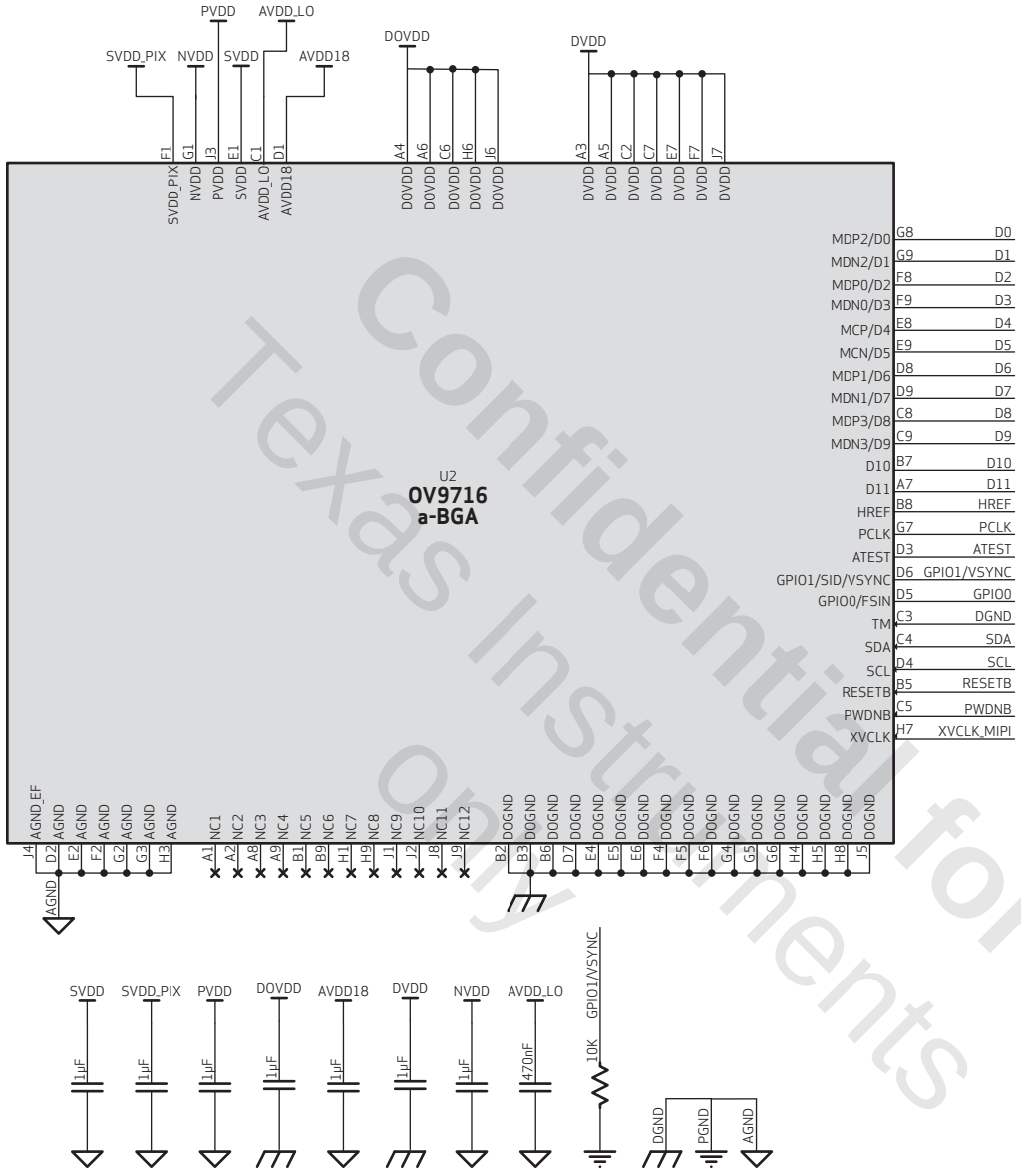


figure 1-5 shows the power supply and signal connection of the OV9716 when using DVP interface.

figure 1-5 OV9716 DVP reference schematic



1.4 power up sequence/ boot sequence

1.4.1 operating modes

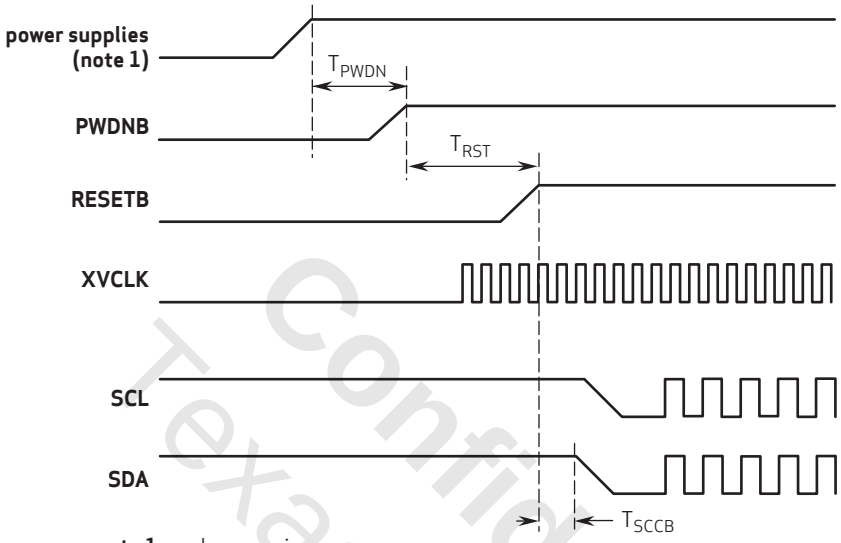
The OV9716 supports the following modes:

- reset mode
  - enabled when RESETB pin low
  - all modules brought to reset, including registers
  - IO pins' states are described according to **table 1-2** (column for RESETB = 0)
  - no active clocks
  - SCCB is disabled
- power down mode (suspend mode)
  - enabled when PWDNB pin low
  - register values are not maintained
  - IOs de-activated (can be tri-stated or driven high or low by register control)
  - clock input is blocked to internal circuit logic control
  - internal clocks stopped
  - all sensor modules powered off, including SCCB
- standby mode
  - asserted after power-up and after SCCB command register 0x3012[0]=0
  - all modules powered ON
  - pads are active
  - PLL stopped
- streaming mode
  - image capture and output streaming enabled

A software reset is required to reset all registers back to their default values. Set register 0x3013[0] and the sensor will be in standby mode after the software reset. It is highly recommended to wait 10ms before programming other registers after a software reset.

1.4.2 power up sequence

figure 1-6 power on timing diagram



note 1 apply power in any sequence

When power is applied to the chip, the analog POR module keeps the chip in reset mode until the voltage is high enough to start operation. When the POR is released, the sensor finishes the hardware reset (HW_RESET) and enters software reset state (SW_RESET) after an additional 9500 XVCLK cycles, during which the sensor loads OTP memory, etc. To extend the HW_RESET period, keep the RESETB pin low. SW_RESET can also be reached from any other state by writing the software reset register bit via SCCB.

T_{SCCB} starts from RESETB going high or when XVCLK is present, whichever is last. The XVCLK must be stable before reset mode is released since reset mode release is clocked by XVCLK. When it is finished, the standby state is reached and the sensor can be programmed over SCCB.

table 1-4 power on timing

parameter	min	max	unit
T_{RST}	1	n/a	ms
T_{SCCB}	9500	n/a	XVCLK cycles

1.4.3 power down sequence

When in standby mode, power down mode can be entered by pulling the PWDNB pin low. In this state, all internal clocks are gated and the internal regulator is set in low-power mode. When the regulator resumes from low power mode, 32767 XVCLK cycles are waited before turning on any clocks to ensure safe operation. Power down mode can only be entered from standby mode.

1.4.4 activation sequence

In standby mode, after setting all registers, including register 0x3012[0]=1, the necessary analog modules and PLLs are turned on. When the PLLs are stable after 4096 XVCLK cycles, the main clocks are switched from XVCLK to the faster PLL clocks, and the integration starts. After the integration period elapses, video data output starts. Note that if the sensor re-enters streaming from standby mode, all registers starting with 0x7000 must be resent before setting 0x3012[0]=1. To save activation time, register settings excluding register 0x3012[0] can also be sent after **section 1.4.5,** deactivation sequence, as long as there is no PWDNB or RESETB pulled down during standby.

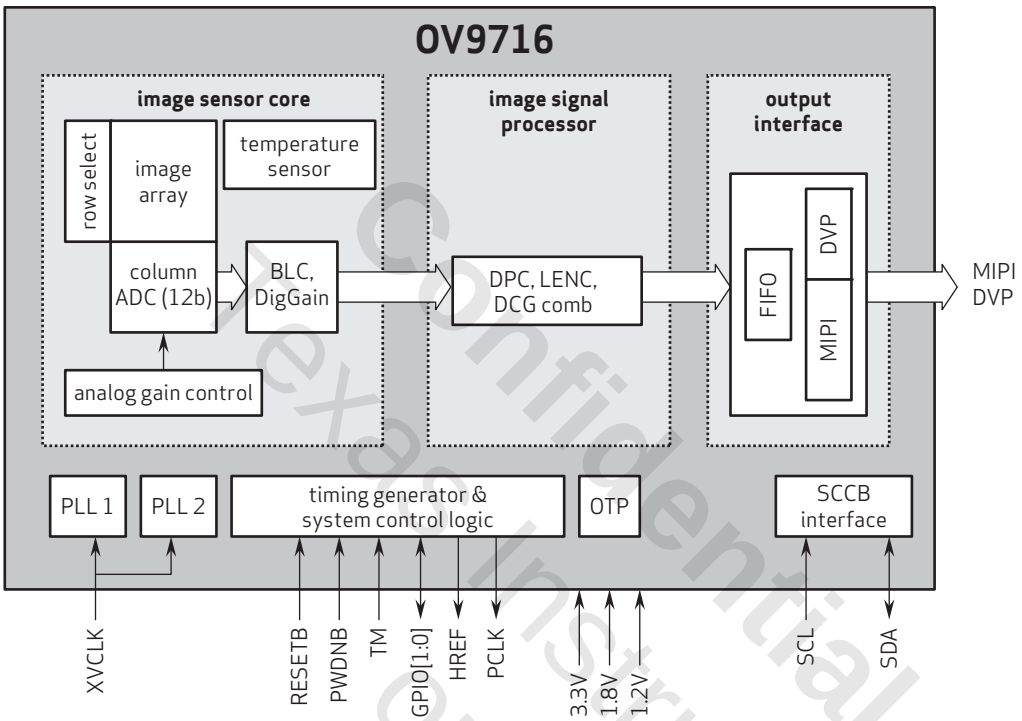
1.4.5 deactivation sequence

In streaming mode, by clearing register 0x3012[0], the chip will enter standby after finishing the current frame (completion is signaled by VSYNC at the DVP-FIFO). The main clock is switched from PLL to XVCLK clock. PLLs and analog modules are turned off. To further reduce the power consumption from the standby state, the PWDNB pin can be pulled low. When this pin is low, the chip is not accessible through the SCCB.

2 sensor architecture

figure 2-1 shows the top level block diagram of the OV9716 sensor.

figure 2-1 OV9716 block diagram



The sensor consists of three major functional blocks: image sensor core, image signal processor (ISP), and output interface.

The image sensor core receives the photo signal which generates electrical charge collected by the pixel photo diodes (PDs). During readout, the accumulated charge is converted to a voltage signal in the pixel. This signal is then amplified and converted to a digital signal by the analog-to-digital converter (ADC). Dark current and circuit offsets are compensated by the black level correction circuit (BLC). The correction is implemented purely in the digital domain. Dark current increases exponentially with temperature and the BLC can be configured to automatically re-trigger with changes in junction temperature, in addition to changes in gain. A temperature sensor is integrated in the image sensor core.

The OV9716 offers dual conversion gain (DCG) HDR, which means the pixels are read out at both low and high conversion gain - low conversion gain (LCG) for large charge handling capacity in the bright portion of the scene, and high conversion gain (HCG) with increased sensitivity and low read noise for the dark portion of the scene. Higher CG means higher sensitivity, as one signal electron can be more easily detected. Higher CG also means that the sensor will realize a reduction in read noise.

The OV9716 also supports staggered very short exposure (VS) to extend the dynamic range to 120 dB. In this mode, HCG and LCG combination can be performed in sensor or in external ISP, however, the DCG and VS combination must be performed in external ISP. The ISP also supports lens shading correction (LENC) and defect pixel correction (DPC).

The processed linear or combined HDR image is formatted and output through the digital video port (DVP) interface or the MIPI interface. Two on-chip phase lock loops (PLLs) generate the required clock signals for all blocks from the XVCLK input clock. The timing generator generates the control signals for the pixel array to reset the PD at the beginning of the exposure, to stop the exposure by reading out the accumulated charge, and also to generate the required control timing for the readout amplifier and ADC. In DVP mode, the horizontal synchronization reference (HREF), vertical synchronization (VSYNC, which can be configured to the GPIO pad), and pixel clock (PCLK) signals are also generated so the backend processor can receive the image data.

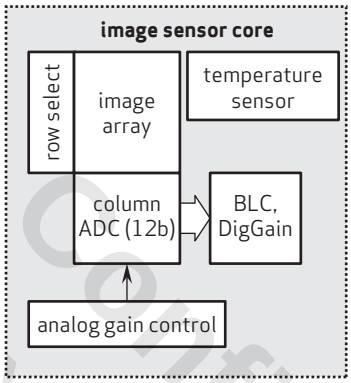
The one time programmable (OTP) memory contains the DPC value and temperature offset value, etc.

All functional blocks are controlled by registers. The host controller can program and read back through the SCCB interface.

3 image sensor core

figure 3-1 shows the top level block diagram of the OV9716 image sensor core.

figure 3-1 sensor core block diagram



The image sensor core consists of the active pixel array, row access control circuit, column parallel analog-to-digital converter (ADC) with gain control, and analog readout channel. A single analog readout channel is used for the processing of three capture channels (HCG, LCG, VS). This provides optimal matching between the capture channels. Gain and BLC are implemented in digital domain.

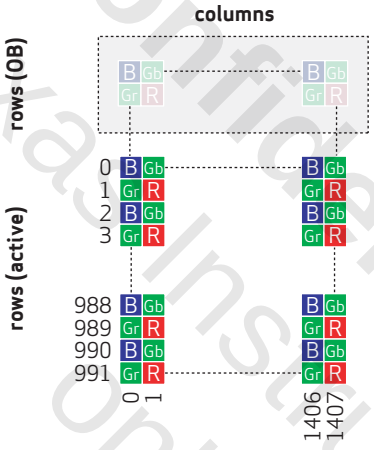
3.1 pixel array structure

The OV9716 sensor has an image array of 1408 columns by 992 rows covered with color filters arranged in a Bayer pattern. **figure 3-2** shows the pixel array color filter layout. In addition to the active pixel rows, optical black (OB) pixel rows are embedded to serve as reference pixels for the black level correction (BLC). The OB rows are covered with a light shield (solid metal layer). In order to minimize non-ideal edge effects in the output image, it is not recommended to use the pixels at the lowest and highest row and column addresses.

The entire readable column is 1392 active columns + 8 active border columns (image quality guarantee) + 8 extra active border columns (no image quality guarantee) = 1408 columns.

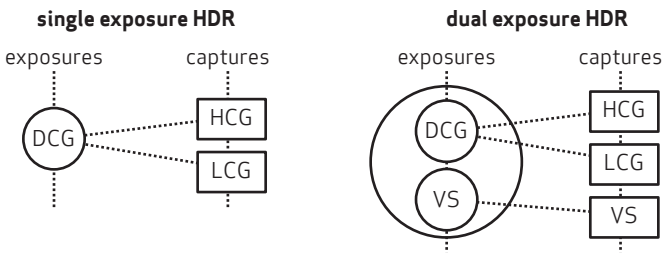
The entire readable row is 976 active rows + 8 active border rows (image quality guarantee) + 8 extra active border rows (no image quality guarantee) = 992 rows.

figure 3-2 pixel array region color filter layout



Each pixel has two switchable conversion gains (CG) to extend the dynamic range. Higher CG (HCG) means higher sensitivity, as one signal electron can be more easily detected. Lower CG (LCG) means lower sensitivity. The OV9716 supports two exposures with three capture readout, with one exposure with two captures in the spatial domain and the shortest exposure in the time domain (see **figure 3-3**).

figure 3-3 exposures and captures diagram



The integration time for VS (T_{VS}) will always start after (T_{HCG}/T_{LCG}) finish. The sampling point is (VS exposure time in rows + 1) rows after, but the T_{VS} start can move from end of T_{HCG}/T_{LCG} to just before sampling of T_{VS} (see **figure 3-4**).

figure 3-4 integration time diagram

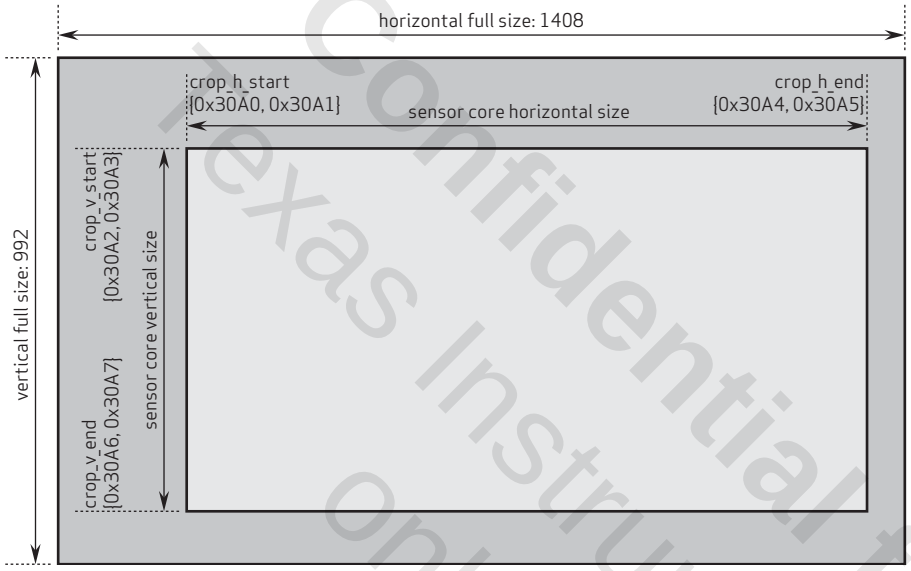
The OV9716 can operate in three modes:

- dual exposure mode: HDR mode with all two exposures, three captures with DCG (HCG and LCG) and VS valid
- single exposure mode: HDR mode with only DCG (HCG and LCG) valid
- linear mode: linear mode using one exposure (HCG or LCG) valid

3.2 pixel array access

The readout window is fully programmable from 256 to 1408 in steps of 4 (8 in sub-sampling) in the horizontal direction and 20 to 992 in steps of 2 (4 in sub-sampling) in the vertical direction. Start address must be at an even row and column and end address must be at an odd row and column address in order to preserve the Bayer pattern order. The crop registers in address 0x30A0~0x30A7 program the sensor core readout window and can be set freely within the pixel array. The start address should always be an even number, while the end address should always be an odd number. The crop window is programmed larger than the processed output image resolution because the ISP uses extra rows and columns for the image processing algorithms (e.g., defect pixel correction).

figure 3-5 pixel array access diagram



3.3 mirror and flip

The pixel array can be accessed in the reverse order in column and row directions (i.e., the image can be horizontally mirrored and vertically flipped (see **figure 3-6**). Image flip is controlled by register 0x30C0[3]. The image mirror setting is shown in **table 3-1**. The sensor needs to be in standby mode when implementing mirror or flip.

table 3-1 register setting for mirror

register name	register address	value
mirror	0x30C0[2]	1
odp_h_offs_l	0x30A9	1
horizontal_output_size_h, horizontal_output_size_l	0x30AC, 0x30AD	crop window size - 2
cfa_pattern	0x3252[0]	1

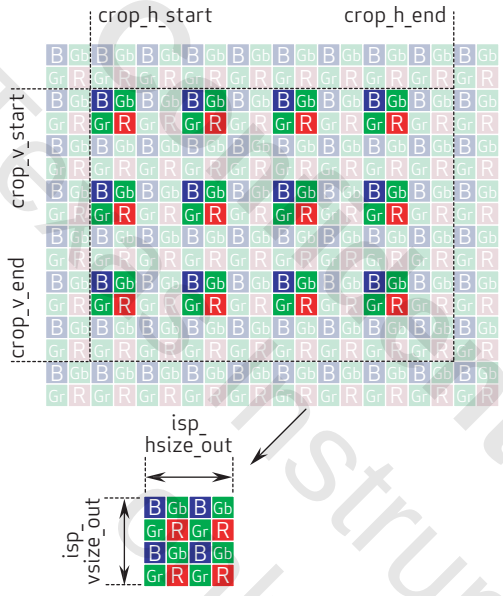
figure 3-6 horizontal mirror and vertical flip samples

original image | mirrored image | flipped image | mirrored and flipped image

3.4 sub-sampling

The pixel array can be sub-sampled by a factor of 2 in both horizontal and vertical directions, controlled by register 0x30BF[1:0]. The sub-sampling is done in the sensor core. The ISP processes the output from the sensor core as a continuous stream of pixel values and generates a lower resolution output image. The horizontal and vertical sub-sampling can be programmed independently. The vertical sub-sampling enables a higher frame rate since the number of rows per frame is reduced, whereas the horizontal sub-sampling will not enable a higher frame rate since the number of clock periods per row is not reduced when horizontal sub sampling is enabled.

figure 3-7 horizontal and vertical sub-sampling

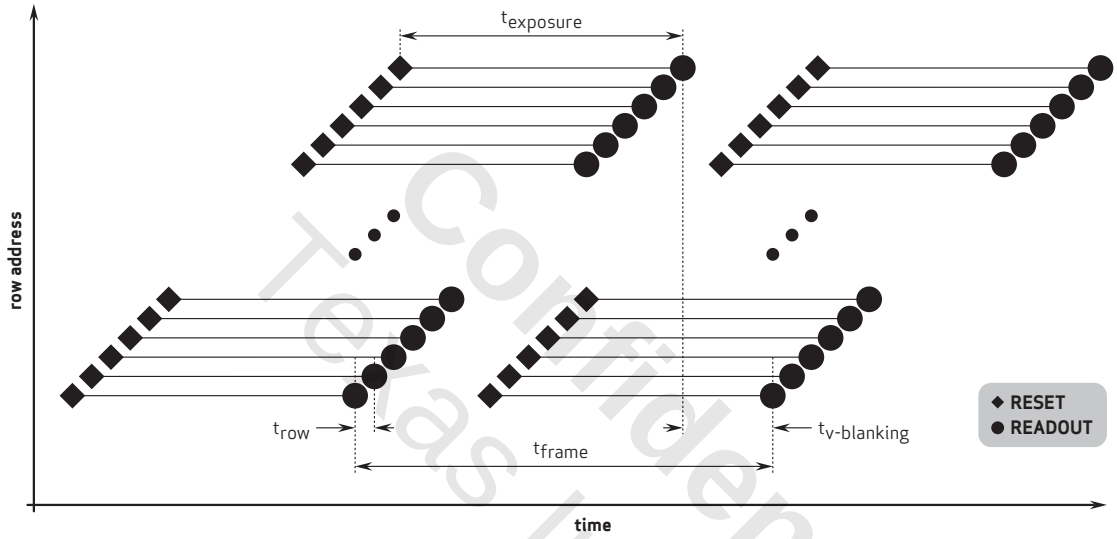


note when using sub-sampling, the size (crop_h_end - crop_h_st+1) and (crop_v_end - crop_v_st + 1) must be multiple of four

3.5 frame timing and maximum frame rate

The OV9716 employs an electronic rolling shutter (ERS) for exposure control (see **figure 3-8**). The pixel array is first reset row by row and when the exposure time has elapsed, the readout of the pixel array is done row by row.

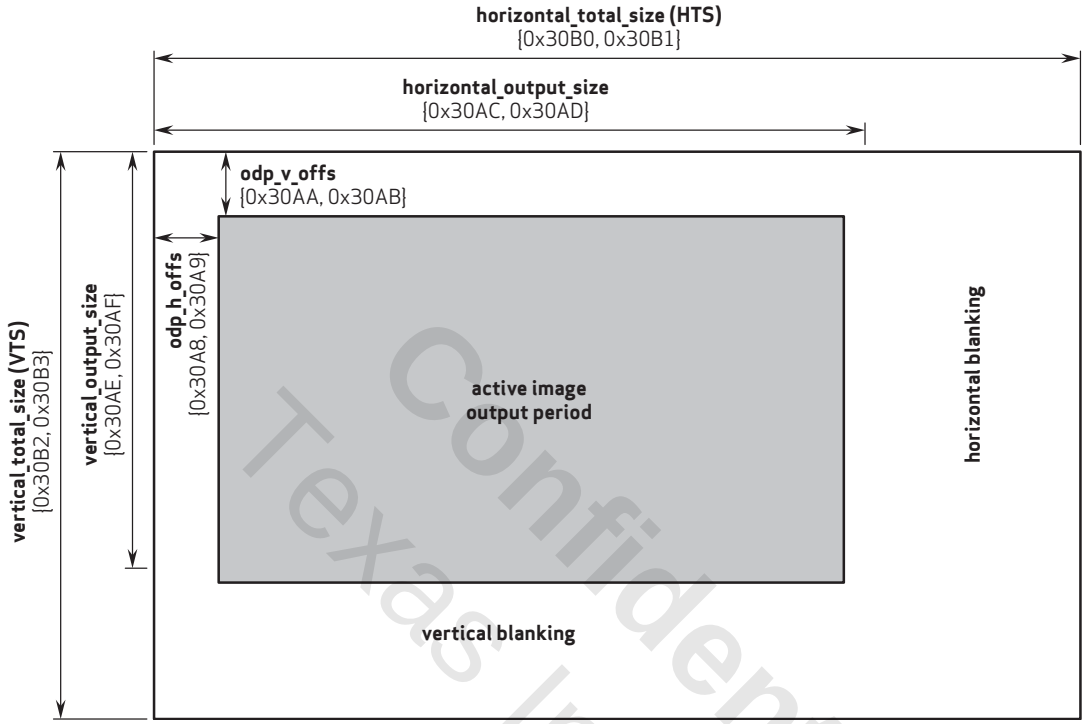
figure 3-8 row address versus time graph



The timing generator generates all the control signals based on a row counter and column counter. Refer to **figure 3-9** for the frame timing. The row period consists of an active output period and a horizontal blanking period. A vertical blanking period is also required to perform frame-based operation. The vertical blanking period seen by the backend processor is usually longer than the internal vertical blanking because the BLC is reading the optical black rows required to perform the correction.

A minimum number of clock periods are required to complete all the required operations per row (blanking time). Refer to **section 5** for details.

figure 3-9 frame output timing diagram



The maximum frame rate is determined by the maximum pixel clock, total number of pixels read out of the entire frame and minimum horizontal/vertical blanking time. The system clock and the minimum blanking time are usually fixed for a given design and the frame rate is dependent on the number of pixels read out. If the requested output image size (ODP size) is smaller than the full pixel array, it is not necessary to read out the whole pixel array, thus; the frame rate can be increased by cropping and/or sub-sampling the pixel array (see **figure 3-4** and **figure 3-7**). Refer to **section 5** output interface for details.

table 3-2 timing control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x30A0	CROP_H_ST_H	0x00	RW	Start Address Horizontal High Byte
0x30A1	CROP_H_ST_L	0x00	RW	Start Address Horizontal Low Byte
0x30A2	CROP_V_ST_H	0x00	RW	Start Address Vertical High Byte
0x30A3	CROP_V_ST_L	0x00	RW	Start Address Vertical Low Byte
0x30A4	CROP_H_END_H	0x05	RW	End Address Horizontal High Byte
0x30A5	CROP_H_END_L	0x7F	RW	End Address Horizontal Low Byte

table 3-2 timing control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x30A6	CROP_V_END_H	0x03	RW	End Address Vertical High Byte
0x30A7	CROP_V_END_L	0xDF	RW	End Address Vertical Low Byte
0x30A8	ODP_H_OFFS_H	0x00	RW	Horizontal Output Offset High Byte
0x30A9	ODP_H_OFFS_L	0x00	RW	Horizontal Output Offset Low Byte
0x30AA	ODP_V_OFFS_H	0x00	RW	Vertical Output Offset High Byte
0x30AB	ODP_V_OFFS_L	0x00	RW	Vertical Output Offset Low Byte
0x30AC	HORIZONTAL_OUTPUT_SIZE_H	0x05	RW	Horizontal Output Size High Byte
0x30AD	HORIZONTAL_OUTPUT_SIZE_L	0x80	RW	Horizontal Output Size Low Byte
0x30AE	VERTICAL_OUTPUT_SIZE_H	0x03	RW	Vertical Output Size High Byte
0x30AF	VERTICAL_OUTPUT_SIZE_L	0xE2	RW	Vertical Output Size Low Byte
0x30B0	HORIZONTAL_TOTAL_SIZE_H	0x08	RW	Horizontal Total Size (HTS) High Byte
0x30B1	HORIZONTAL_TOTAL_SIZE_L	0x0A	RW	Horizontal Total Size (HTS) Low Byte
0x30B2	VERTICAL_TOTAL_SIZE_H	0x03	RW	Vertical Total Size (VTS) High Byte
0x30B3	VERTICAL_TOTAL_SIZE_L	0xF4	RW	Vertical Total Size (VTS) Low Byte
0x30B4	EXTRA_DELAY_H	0x00	RW	Last Row Can Be Extended By This Number of Clocks (fs_delay), High Byte Auto-reset to 0 if 0x30BD[0] is set. Applied to frame N+2.
0x30B5	EXTRA_DELAY_L	0x00	RW	Last Row Can Be Extended By This Number Of Clocks (fs_delay), Low Byte Auto-reset to 0 if 0x30BD[0] is set. Applied to frame N+2.

3.6 exposure control

The OV9716 has two exposure and channel: DCG (HCG or LCG) and VS. Their exposure time can be set manually in registers:

- minimum exposure is one line
- maximum exposure is VTS -2 lines
- {0x30B6[7:0], 0x30B7[7:0]} for DCG (HCG or LCG) exposure time
- {0x30B8[7:0], 0x30B9[7:0]} for VS exposure time

All exposure time values are represented by the unit of row time:

$$T_{ROW} = HTS \times Tsclk = \frac{HTS}{Fsclk}$$

where Tsclk is the system clock period and Fsclk is the system clock frequency.

The actual exposure time value of the current frame can be read back from 0x30C9[7:0]~0x30CA[7:0] for DCG (HCG or LCG), 0x30CB[7:0]~0x30CC[7:0] for integer part of VS. Since 0x30B6~0x30B9 will take effect at N+2 frame, user can get the exposure time value for current frame with 0x30C9~0x30CC.

The OV9716 has a restriction for changing VS exposure time. If deltaVS is negative (VS exposure time is reduced), it will be limited as following:

$$\text{max\_neg\_deltaVS} = \text{vts} - \left(17 + \text{Odp\_v\_size} + \frac{\text{Odp\_v\_offset}}{(1+\text{Vsub2})} + 2 * \text{show\_emb\_rows}\right)$$

where VTS is the vertical total size {0x30B2, 0x30B3}. Vsub2 is the sub-sampling defined by 0x30BF[1]. vertical_output_size is the output data path vertical size {0x30AE, 0x30AF}, odp_v_offset is the output data path vertical offset {0x30AA, 0x30AB}, show_emb_rows is the switch to enable/disabled embedded rows {0x30C1[2]}. VS exposure time can never be reduced faster than max_neg_deltaVS. If deltaVS is defined larger than the max_neg_deltaVS, the sensor will automatically reduce VS exposure time with max_neg_deltaVS frame by frame gradually until target VS exposure time has been reached.

For example, if the sensor has the following settings in dual exposure mode:

- vertical_output_size = 994; odp_v_offset = 0
- VTS = 1020
- no sub sampling
- no embedded row (0x30C1[2] = 0)
- max_neg_deltaVS = 1020 - (17 + 994 + (0/(1+0)) - 2*0) = 9

If VS exposure time is changed from 40 to 10, VS exposure time will change like this:

- Frame0: VS exposure time = 40
- Frame1: VS exposure time = 31 (deltaVS = -9)
- Frame2: VS exposure time = 22 (deltaVS = -9)

- Frame3: VS exposure time = 13 (deltaVS = -9)
- Frame4: VS exposure time = 10 (deltaVS = -3, target VS exposure time reached)

The exposure control is double frame-synced, which means that a change in the setting of the current frame (N) will take place. The actual exposure will change on the second frame after (at N+2). This period is fixed and cannot be adjusted.

table 3-3 exposure control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x30B0	HORIZONTAL_ TOTAL_SIZE_H	0x08	RW	Horizontal Total Size (HTS) High Byte
0x30B1	HORIZONTAL_ TOTAL_SIZE_L	0x0A	RW	Horizontal Total Size (HTS) Low Byte
0x30B2	VERTICAL_TOTAL_ SIZE_H	0x03	RW	Vertical Total Size (VTS) High Byte
0x30B3	VERTICAL_TOTAL_ SIZE_L	0xF4	RW	Vertical Total Size (VTS) Low Byte
0x30B4	EXTRA_DELAY_H	0x00	RW	Last Row can be Extended by This Number of Clocks (fs_delay), High Byte Auto-reset to 0 if 0x30BD[0] is set. Applied to frame N+2.
0x30B5	EXTRA_DELAY_L	0x00	RW	Last Row can be Extended by This Number of Clocks (fs_delay), Low Byte Auto-reset to 0 if 0x30BD[0] is set. Applied to frame N+2.
0x30B6	CEXP_DCG_H	0x00	RW	Frame DCG (HCG/LCG) Exposure (in Rows)
0x30B7	CEXP_DCG_L	0x10	RW	Frame DCG (HCG/LCG) Exposure (in Rows)
0x30B8	CEXP_VS_H	0x00	RW	Frame Very Short Exposure (in Rows)
0x30B9	CEXP_VS_L	0x02	RW	Frame Very Short Exposure (in Rows)
0x30BB	CG_AGAIN	0x00	RW	Conversion Gains and Analog Gains Bit[7]: cg_vs Very short conversion gain Bit[5:4]: again_vs Very short analog gain Bit[3:2]: again_lcg LCG analog gain Bit[1:0]: again_hcg HCG
0x30BC	EXTRA_VTS	0x00	RW	Delay Added to VTS (in rows) Auto-reset to 0 if 0x30BD[0] is set. Applied to frame N+2 unless 0x30BD[2] is set.

table 3-3 exposure control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x30BF	SKIP_CTRL	0x00	RW	Bit[2]: Monochrome Monochrome readout mode Bit[1]: Vsub2 Skip 2/2 rows or 1/1 rows in monochrome mode Bit[0]: Hsub2 Skip 2/2 columns or 1/1 columns in monochrome mode
0x30C0	READ_MODE	0x80	RW	Bit[7]: always_active_dp When high, data path will stay active also when there are no valid data to process Bit[6]: align_buf_flip Flip order of align buffer readout trigger 0: VS is last 1: L is last Bit[5:4]: multi_samp Multisampling for L 00: 1 01: 2 10: 4 11: Undefined Bit[3]: Flip Reverse row readout order Bit[2]: Mirror Reverse column readout order Bit[0]: align_repeat_last_row When set, repeat last row for invalid rows when always_active_dp is set
0x30C9	EXP_DCG_H	–	R	Current Frame DCG (HCG/LCG) Exposure Time (in Rows) High Byte
0x30CA	EXP_DCG_L	–	R	Current Frame DCG (HCG/LCG) Exposure Time (in Rows) Low Byte
0x30CB	EXP_VS_H	–	R	Current Frame Very Short Exposure Time (in Rows) High Byte
0x30CC	EXP_VS_L	–	R	Current Frame Very Short Exposure Time (in Rows) Low Byte
0x30CD	EXP_VS_F	–	R	Current Frame Fractional Very Short Exposure (Actual Adjusted Value)

When cropping window is changed from a lower address to a higher address in the vertical direction, exposure must be limited to be equal or less than VTS - (crop_start_new - crop_start_old) - 1. Otherwise, there will be two corrupt frames. Gain can be added to maintain the same brightness during the transition.

3.7 gain control

3.7.1 conversion gain (linear mode only)

Conversion gain is controlled by register 0x30BB[6], where '1' means high conversion gain and '0' means low conversion gain.

3.7.2 analog gain (up to 8x)

3.7.2.1 HDR mode

table 3-4 HDR analog gain registers

address	function
0x30BB[5:4]	VS 00: 1x 01: 2x 10: 4x
0x30BB[3:2]	LCG 00: 1x 01: 2x 10: 4x
0x30BB[1:0]	HCG 00: 1x 01: 2x 10: 4x

3.8 black level calibration (BLC)

The black level correction (BLC) function is used to set the pixel output of a complete black object to a programmable pedestal value in all kinds of lightning conditions. Due to circuit offset and pixel dark current, the pixel output level of a black object is normally non-zero. The OV9716 calibrates the black level of the active pixel by subtracting the true optical black pixel output.

The target BLC pedestal value for HCG, LCG, and VS channels are set by registers {0x3168, 0x3169}, {0x316A, 0x316B}, and {0x316C, 0x316D}, respectively. The pedestals are 12-bit values. The ISP will subtract the pedestal value early in the signal processing path.

When the BLC is enabled, the active pixel output value will be limited to 0xFFF after subtracting the optical black pixel value. The BLC value can be manually overridden enabled by the registers 0x3140[4] for HCG, 0x3140[5] for LCG and 0x3140[6] for VS. In this case, the BLC function is disabled.

3.8.1 advanced operation of the BLC

The BLC is based on measuring the value at the center of the distribution of the optical black reference pixels and applying digital correction to bring the center to the predefined target value. The center of the pixel distribution is estimated from a combination of median and average filtering. The filtering for the BLC is based on the middle 1024 columns of the 8 optical dark rows. Only the values closest to the horizontal center of each row are used in order to minimize influence from any edge effects in the array.

During normal operation, dark current is expected to change slowly with time. During slow changes, the BLC in the OV9716 will not change the correction value before a certain delta is measured. This triggering is configurable in the blc_trigger_threshold registers for HCG, LCG, and VS exposures in registers {0x3154, 0x3155}, {0x3156, 0x3157}, and {0x3158, 0x3159} respectively. When one of these thresholds is crossed, the correction value is updated with an exponential moving average smoothing filter. The fractional smoothing factor is configurable in 0x3141 and affects the α in:

$$correction_{FILTER} = correction_{LAST} + \alpha \times (correction_{NEW} - correction_{LAST}),\ 0 \le \alpha \le 1$$

α is encoded as a 5-bit register value, so that α = (smoothing+1)/32. Setting smoothing to 0 means that no update is applied, while setting smoothing to 31 means that the new value is directly applied without smoothing.

Continuously updating the correction values in BLC may lead to undesired flickering, hence BLC trigger-mode is implemented. When BLC is in trigger-mode, the correction values remain unchanged until a condition (trigger) occurs. There are multiple sources of triggers for the BLC:

- restart frame triggering
- exposure changed triggering
- gain changed triggering
- threshold triggering
- manual triggering (register write)

When triggered, the correction values in BLC are updated continuously in a number of frames determined by restart_frames register (0x315E). Two kinds of responses can be taken:

- Hard trigger, where the first frame is applied directly (no filtering), while restart_frames registers are run with filtering. If direct application is wanted for all restart_frames, set smoothing to maximum.
- Soft trigger, where blc_restart_frames are applied with filtering.

Restart frame, exposure or gain changed are always hard triggers. Threshold and manual triggers can be either hard or soft. There are two thresholds for each exposure. The hard threshold will always cause a hard trigger while the main threshold can be programmed to be soft or hard. A trigger will always cause BLC for all exposures to be triggered. It is assumed that the VS exposure is later than the DCG exposure when triggered, ensuring that the VS exposure BLC is triggered in the same frame as the DCG exposure.

Threshold triggering occurs when the absolute difference between current measured dark level and currently applied dark level is larger than a configurable amount. All three captures are monitored and can cause a threshold trigger.

If triggering is not enabled, the correction values are updated in every frame. When filtering is enabled, the correction value is still directly applied upon a hard trigger.

After a trigger, it is possible to have the BLC soft-triggered for a number of frames, restart_frames register (0x315E). This can help average noise over multiple frames after a hard trigger.

It is possible to disable the threshold crossed triggers by writing the blc_trigger_threshold registers to 0xFF. It is also possible to handle the threshold crossed triggers as hard triggers by setting the 0x3153[1] bit to 1.

Manual triggering is possible by writing a 1 to the 0x3153[0] bit. Note that this bit must be manually cleared. To manually cause a hard-trigger, the 0x3153[1] bit must also be set.

The maximum correction value can be programmed by registers blc_max_correction (0x3160 and 0x3161).

The pedestal values (blc_target_*) are also double frame-synced, thus any change that is being imposed during a frame (N), is going to start to take effect two frames after (at N+2). The same applies for analog and digital gain settings. The time period is fixed and cannot be adjusted.

table 3-5 BLC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3140	BLC_CTRL	0x02	RW	Bit[6:4]: blc_override_en Use manual BLC values from blc_override_* registers. Separate enable for HCG (Bit[4]), LCG (Bit[5]) and VS (Bit[6]) exposures Bit[3]: blc_cont_update_mode Enable BLC recalculation on every frame Bit[1]: blc_dither_en Enable dithering on unused sub-LSBs of incoming data Bit[0]: show_dark_rows Show dark rows in image

table 3-5 BLC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x314C	BLC_OVERRIDE_HCG_H	0x00	RW	Manual BLC Override Value for HCG Exposure High Byte
0x314D	BLC_OVERRIDE_HCG_L	0x00	RW	Manual BLC Override Value for HCG Exposure Low Byte
0x314E	BLC_OVERRIDE_LCG_H	0x00	RW	Manual BLC Override Value for LCG Exposure High Byte
0x314F	BLC_OVERRIDE_LCG_L	0x00	RW	Manual BLC Override Value for LCG Exposure Low Byte
0x3150	BLC_OVERRIDE_VS_H	0x00	RW	Manual BLC Override Value for VS Exposure High Byte
0x3151	BLC_OVERRIDE_VS_L	0x00	RW	Manual BLC Override Value for VS Exposure Low Byte
0x3152	FRAME_FILTER_CTRL	0x04	RW	Frame Filter Control Bit[2]: frfilt_old_value_select Select 'old' dark level value to be used in alpha filter 0: Official 'last dark level' 1: Stored filter output from previous frame Bit[1]: frfilt_hard_thres_mux_select Input to delta-computation in front of hard threshold comparator is dark level value 0: After alpha filter 1: Before alpha filter Bit[0]: frfilt_main_thres_mux_select Input to delta-computation in front of main threshold comparator is dark level value 0: After alpha filter 1: Before alpha filter
0x315F	AB_CTRL	0x00	RW	Controls AB Mode Operation (Bit[0] Must Be Set and Bit[1] Must Be Toggled, 0: A Frame, 1: B Frame) Bit[7:6]: blc_raw_sel 00: HCG 01: LCG 10: VS 11: Not used Bit[1]: Bframe Selects between A (0) and B (1) frames Bit[0]: ab_mode Enable AB mode

table 3-5 BLC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3160	BLC_MAX_CORRECTION_H	0x0F	RW	Maximum Value of BLC Correction High Byte
0x3161	BLC_MAX_CORRECTION_L	0xFF	RW	Maximum Value of BLC Correction Low Byte
0x3162	DIG_GAIN_HCG_H	0x01	RW	Digital Gain for HCG (Format 6.8) High Byte
0x3163	DIG_GAIN_HCG_L	0x00	RW	Digital Gain for HCG (Format 6.8) Low Byte
0x3164	DIG_GAIN_LCG_H	0x01	RW	Digital Gain for LCG (Format 6.8) High Byte
0x3165	DIG_GAIN_LCG_L	0x00	RW	Digital Gain for LCG (Format 6.8) Low Byte
0x3166	DIG_GAIN_VS_H	0x01	RW	Digital Gain for VS (Format 6.8) High Byte
0x3167	DIG_GAIN_VS_L	0x00	RW	Digital Gain for VS (Format 6.8) Low Byte
0x3168	BLC_TARGET_HCG_H	0x00	RW	Black Level Target HCG Exposure High Byte
0x3169	BLC_TARGET_HCG_L	0x40	RW	Black Level Target HCG Exposure Low Byte
0x316A	BLC_TARGET_LCG_H	0x00	RW	Black Level Target LCG Exposure High Byte
0x316B	BLC_TARGET_LCG_L	0x40	RW	Black Level Target LCG Exposure Low Byte
0x316C	BLC_TARGET_VS_H	0x00	RW	Black Level Target VS Exposure High Byte
0x316D	BLC_TARGET_VS_L	0x40	RW	Black Level Target VS Exposure Low Byte
0x316F	DIG_GAIN_FS2_HCG_L	–	R	Readback of Frame Synchronized Digital Gain for HCG Exposure Low Byte
0x3170	DIG_GAIN_FS2_LCG_H	–	R	Readback of Frame Synchronized Digital Gain for LCG Exposure High Byte
0x3171	DIG_GAIN_FS2_LCG_L	–	R	Readback of Frame Synchronized Digital Gain for LCG Exposure Low Byte
0x3172	DIG_GAIN_FS2_VS_H	–	R	Readback of Frame Synchronized Digital Gain for VS Exposure High Byte
0x3173	DIG_GAIN_FS2_VS_L	–	R	Readback of Frame Synchronized Digital Gain for VS Exposure Low Byte
0x3174	BLC_TARGET_FS2_HCG_H	–	R	Readback of Black Level Target HCG Exposure High Byte
0x3175	BLC_TARGET_FS2_HCG_L	–	R	Readback of Black Level Target HCG Exposure Low Byte
0x3176	BLC_TARGET_FS2_LCG_H	–	R	Readback of Black Level Target LCG Exposure High Byte
0x3177	BLC_TARGET_FS2_LCG_L	–	R	Readback of Black Level Target LCG Exposure Low Byte

table 3-5 BLC control registers (sheet 4 of 4)

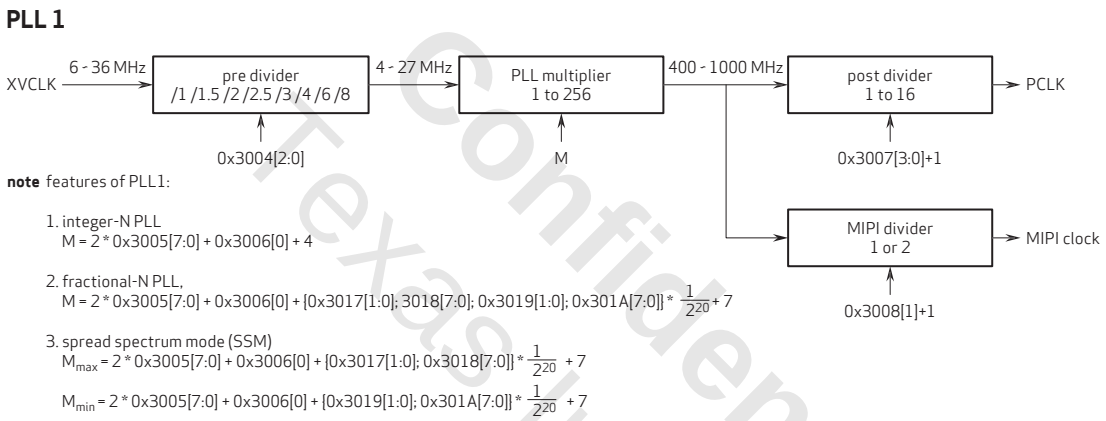
address	register name	default value	R/W	description
0x3178	BLC_TARGET_FS2_VSH	–	R	Readback of Black Level Target VS Exposure High Byte
0x3179	BLC_TARGET_FS2_VSL	–	R	Readback of Black Level Target VS Exposure Low Byte
0x317A	DARK_CURRENT_HCG_H	–	R	Dark Current Compensation for HCG Exposure (Signed) High Byte
0x317B	DARK_CURRENT_HCG_L	–	R	Dark Current Compensation for HCG Exposure (3 Sub-LSBs) Low Byte
0x317C	DARK_CURRENT_LCG_H	–	R	Dark Current Compensation for LCG Exposure (Signed) High Byte
0x317D	DARK_CURRENT_LCG_L	–	R	Dark Current Compensation for LCG Exposure (3 Sub-LSBs) Low Byte
0x317E	DARK_CURRENT_VS_H	–	R	Dark Current Compensation for VS Exposure (Signed) High Byte
0x317F	DARK_CURRENT_VS_L	–	R	Dark Current Compensation for VS Exposure (3 Sub-LSBs) Low Byte
0x3180	ROW_AVERAGE_HCG_H	–	R	Row Average (Accumulator Value) for HCG Exposure (Signed) High Byte
0x3181	ROW_AVERAGE_HCG_L	–	R	Row Average (Accumulator Value) for HCG Exposure (3 Sub-LSBs) Low Byte
0x3182	ROW_AVERAGE_LCG_H	–	R	Row Average (Accumulator Value) for LCG Exposure (Signed) High Byte
0x3183	ROW_AVERAGE_LCG_L	–	R	Row Average (Accumulator Value) for LCG Exposure (3 Sub-LSBs) Low Byte
0x3184	ROW_AVERAGE_VS_H	–	R	Row Average (Accumulator Value) for VS Exposure (Signed) High Byte
0x3185	ROW_AVERAGE_VS_L	–	R	Row Average (Accumulator Value) for VS Exposure (3 Sub-LSBs) Low Byte
0x318F	BFRAME_FS2	–	R	Readback of Frame Synchronized Bframe Bit from ab_ctrl register

3.9 PLL

PLL settings can only be changed during sensor standby mode (0x3012 = 0).

The OV9716 implements two PLLs with both inputs connected to the XVCLK pin. One can support the MIPI bit clock and output clock PCLK, while the other one can support internal SCLK. Two PLLs enable the internal clock (SCLK) to be separate from the output clock (PCLK). Additionally, in MIPI mode, the two PLLs can be used to optimize the MIPI frequency to minimize EMI.

figure 3-10 PLL1 control diagram



In order to reduce EMI's impact, this PLL also supports spread spectrum mode (SSM). Spread profile is a triangular waveform spread. The spectrum can be up spread, both side spread, or down spread depend on the input setting dsm[19:0]. Tssc is the modulation period. Fssc(1/Tssc) is the modulation frequency, which is about 30KHz~33KHz. DeltaF is modulation amplitude, which is normally smaller than 5000ppm. For example, if normal clock frequency Fo=1GHz, then 5000ppm=5000×Fo/1e6=5MHz.

$$Fmax = \frac{RefClk}{PreDiv} \cdot [2 * pdiv[7:0] + 7 + sdiv + dsm[19:10] \cdot (\frac{1}{2^9})]$$

$$Fmin = \frac{RefClk}{PreDiv} \cdot [2 * pdiv[7:0] + 7 + sdiv + dsm[9:0] \cdot (\frac{1}{2^9})]$$

figure 3-11 PLL2 control diagram

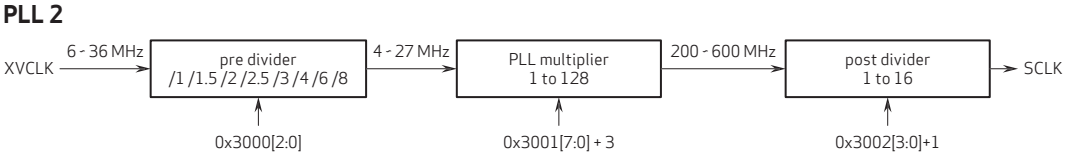


table 3-6 PLL control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3000	SCLK_PLL_PRE	0x05	RW	SCLK PLL Pre Divider
0x3001	SCLK_PLL_MULT	0x60	RW	SCLK PLL Multiplier VCO Frequency Multiplier Is sclk_pll_mult+3
0x3002	SCLK_PLL_POST	0x03	RW	SCLK PLL Post Divider (1-16)
0x3003	SCLK_PLL_CONFIG	0x01	RW	Bit[7:6]: lock_precision Lock detector precision resolution setting Bit[5:4]: lock_cntref Lock detector counter setting Bit[3]: fastlock_disable 0: Enable fast locking 1: Disable fast locking Bit[2:0]: Cp Charge pump current
0x3004	PCLK_PLL_PRE	0x06	RW	PCLK PLL Pre Divider
0x3005	PCLK_PLL_PDIV	0x7B	RW	PCLK PLL Core Loop Div 1 (1-256)
0x3006	PCLK_PLL_SDIV	0x00	RW	PCLK PLL Core Loop Div 2
0x3007	PCLK_PLL_POST	0x07	RW	PCLK PLL Post Divider (1-16)
0x3008	PCLK_PLL_CTRL1	0x01	RW	PCLK and SCLK PLL Control 1 Bit[5]: sclk_pll_bypass Bypass PLL2 clock within PLL Bit[4]: sclk_pll_enable Enable PLL2 (SCLK) Bit[2]: pclk_pll_bypass Bypass PLL1 clock within PLL Bit[1]: pclk_pll_mipi_div Divide frequency to MIPI by 2 Bit[0]: pclk_pll_enable Enable PLL1 (PCLK)
0x3009	PCLK_PLL_CTRL2	0x00	RW	PCLK PLL Control 2 Bit[6:5]: ssc_cntstep Select SSC counter step number Bit[4:2]: ssc_cntck Set SSC counter frequency Bit[1]: ssc_en Enable SSC mode Bit[0]: frac_en Enable fractional mode

table 3-6 PLL control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3017	PCLK_PLL_DSM_MAX_H	0x00	RW	PCLK PLL Fractional Div[19:18] (SSC Maximum High Byte)
0x3018	PCLK_PLL_DSM_MAX_L	0x00	RW	PCLK PLL Fractional Div[17:10] (SSC Maximum Low Byte)
0x3019	PCLK_PLL_DSM_MIN_H	0x00	RW	PCLK PLL Fractional Div[9:8] (SSC Minimum High Byte)
0x301A	PCLK_PLL_DSM_MIN_L	0x00	RW	PCLK PLL Fractional Div (SSC Minimum Low Byte)
0x301B	PCLK_PLL_CONFIG	0x01	RW	Bit[7:6]: lock_precision Lock detector precision resolution setting Bit[5:4]: lock_cntref Lock detector counter setting Bit[3]: fastlock_disable 0: Enable fast locking 1: Disable fast locking Bit[2:0]: CP Charge pump current Current = 5*(cp+1)

3.10 temperature sensor

The OV9716 has an embedded temperature sensor in image sensor core to measure junction temperature. The temperature sensor is enabled by register {0x3066}. The temperature can be read back by registers {0x3067, 0x3068}. The value will be in Celsius. Please note that if 0x3067[0] = 0, directly convert the numbers in 0x3068 from hex to decimal. If 0x3067[0] = 1, retrieve the 2's complement numbers of register 0x3068 first and then convert the numbers to decimal. The slope and offset of the temperature sensor is calibrated in an OmniVision production test and the calibration data is stored in the OTP. After calibration, the accuracy of the temperature reading is ± 7°C over 60°C to 105°C. Out of this range, reading from the temperature sensor is not reliable and is for reference only.

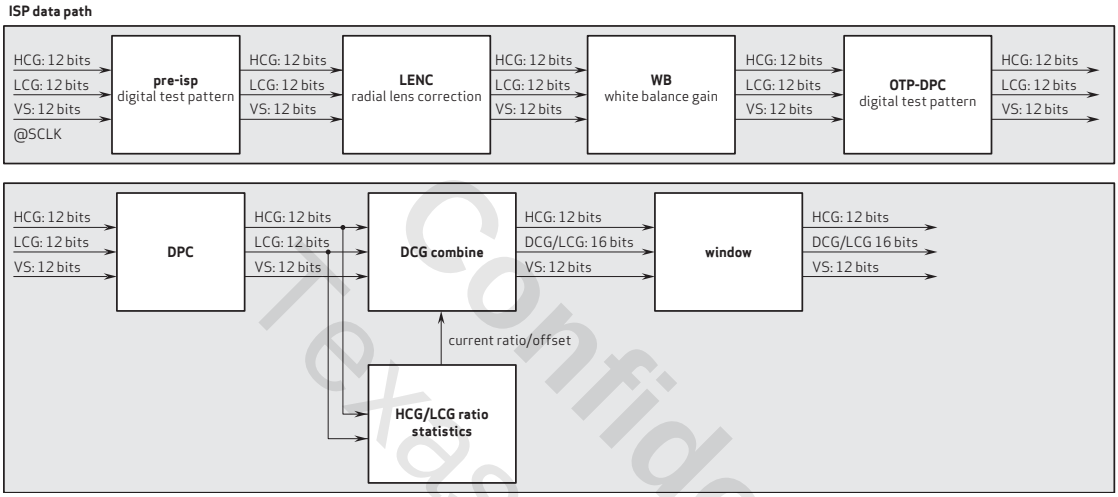
table 3-7 temperature sensor registers

address	register name	default value	R/W	description
0x3066	TS_CTRL	0x80	RW	Bit[7]: ts_en Enable temperature sensor Bit[6]: ts_standby_en Enable temperature sensor in standby
0x3067	TS_RD_H	–	R	Temperature Read Out C Degrees, Sign Bit
0x3068	TS_RD_L	–	R	Temperature Read Out C Degrees, Signed Low Byte

4 image processor

figure 4-1 shows the top level block diagram of the OV9716 image processor.

figure 4-1 image processor block diagram



The ISP receives image data from the sensor core and includes modules for RAW image processing. The video stream arrives as 12-bit parallel data separated in high conversion gain (HCG), low conversion gain (LCG) and very short (VS) exposure channels. Unused rows and columns are cut before further processing. After processing the data from the ISP, it is configured to the correct output format in the output interface.

One of the first processing steps in the ISP is to correct the shading caused by lens fall off (LENC). Digital gain is then applied to make the image white balanced (WB gain). Defect pixel and clusters (DPC) are corrected on-the-fly for each captures. After that the DCG exposures (HCG and LCG) are combined into a 16-bit HDR image (DCG combine). In the transition area, the data is linearly combined.

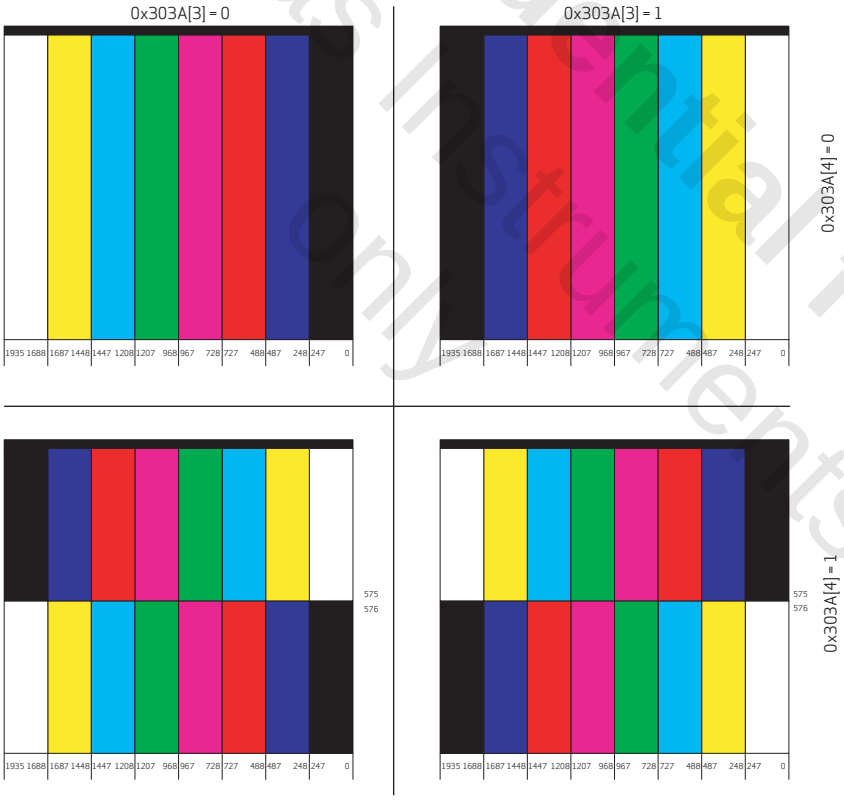
4.1 test pattern

For testing purposes, the OV9716 offers analog and digital test patterns. The analog test pattern is a color bar overlaid with pixel output to excise the whole analog readout channel. It can be enabled by setting register 0x303A[5] to 1. The intensity of this color bar can be controlled by register 0x303A[2:0] and the order of colors can be swapped by setting register 0x303A[3] = 1. The OV9716 also offers two digital effects for the test patterns: transparent effect and rolling bar effect. The digital test pattern function is enabled by register 0x3253[7] and the test pattern is selected by register 0x3253[6:0]. The test patterns are only available if the ISP is enabled (0x3250[0] = 1). The test patterns are processed by the ISP and outputted as regular images. The input data of test pattern is unaffected by sensor exposure time and gain, however, the ISP processing parameters may be still dependent on the gain.

4.1.1 analog color bar overlay

The analog color bar overlay is enabled by setting register 0x303A[5] = 1, the overlay patterns are selected by programming 0x303A[4:3] (see **figure 4-2**) and the color intensity is adjusted by programming register 0x303A[2:0]. **figure 4-2** also shows how the color bar patterns are mapped to the physical row and column addresses. The location of the mid-array rows, where the patterns are swapped, as well as the color bar borders, remain the same regardless if the image is cropped or not.

figure 4-2 color bar types



4.1.2 digital test patterns

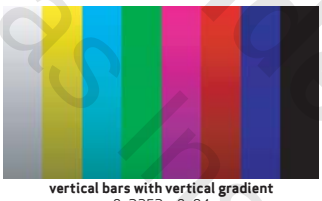
Before enabling the digital test patterns, it must be ensured, that the used sensor core vertical size (crop_v_end - crop_v_start) has at least two more rows compared to the output data path vertical size (vertical_output_size), and that the output data path vertical offset (odp_v_offs) is utilized with a value of at least 2.

The data path test patterns are only available if the ISP is enabled (0x3250[0] = 1). The test patterns are processed by the ISP and outputted as regular images. However, they are unaffected by sensor exposure time and digital gain.

figure 4-3 vertical bars test pattern

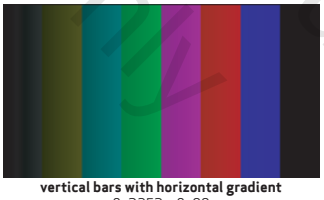
vertical bars
0x3253 = 0x80

figure 4-4 vertical bars with vertical gradient test pattern



vertical bars with vertical gradient
0x3253 = 0x84

figure 4-5 vertical bars with horizontal gradient test pattern

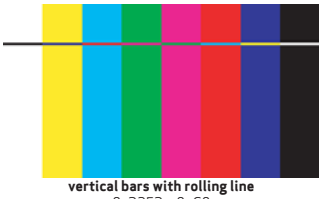


vertical bars with horizontal gradient
0x3253 = 0x88

figure 4-6 vertical bars with diagonal gradient test pattern

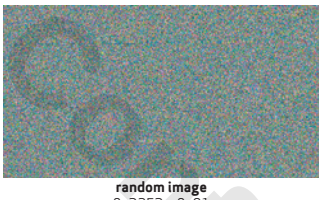
vertical bars with diagonal gradient
0x3253 = 0x8C

figure 4-7 vertical bars with rolling line test pattern



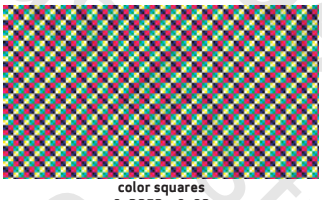
vertical bars with rolling line
0x3253 = 0xC0

figure 4-8 random image test pattern



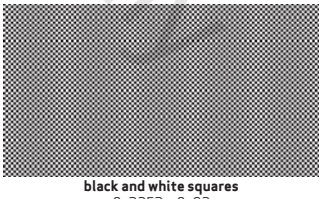
random image
0x3253 = 0x81

figure 4-9 color squares test pattern



color squares
0x3253 = 0x82

figure 4-10 black and white squares test pattern



black and white squares
0x3253 = 0x92

figure 4-11 chart test pattern

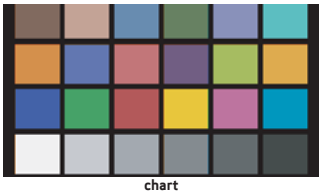


chart
0x3253 = 0x83

table 4-1 test pattern control registers

address	register name	default value	R/W	description
0x303A	ANA_CB	0x04	RW	Bit[5]: cb_en Enable color bars Bit[4]: cb_mode 0: Do not swap color bars mid-array 1: Swap color bars mid-array (mirror rows) Bit[3]: cb_swap 0: Do not swap color bars 1: Swap color bars (mirror columns) Bit[2:0]: cb_adjust ICB current level (color bar intensity)
0x3250	ISP_DP_CONF1	0x33	RW	ISP Datapath Configuration (Module Bypass/Enable) Bit[7]: dpc_bc_en Black pixel correction enable in DPC Bit[6]: dpc_wc_en White pixel correction enable in DPC Bit[5]: isp_out_window_en ISP output window crop enable Bit[4]: comb_en DCG combine enable Bit[3]: lenc_en Lens correction enable Bit[2]: otp_en Defect pixel tagging enable Bit[1]: wb_gain_en WB gain enable Bit[0]: isp_en ISP enable

4.2 lens correction (LENC)

The first step in the image processing pipeline is to correct the shading due to light fall off in the edges and corner areas. The correction is done by multiplying each pixel with a gain based on the area where each pixel is located. The control points are separated for red, green and blue (see registers 0x3330~0x3347). LENC is disabled by default and can be enabled by register 0x3250[3].

The OV9716 supports sub-sampling and flip in both horizontal and vertical directions while LENC is enabled.

The LENC control registers are separate for red, green and blue.

Under dark conditions, the signal-to-noise ratio (SNR) drops in the corner areas. The noise can be significantly amplified by the lens correction gain and results in a brighter corner. The OV9716 can automatically adjust gain for the pixels to adapt to lighting conditions. This is accomplished by following the sensor analog gain and is enabled through register 0x3348[2].

LENC uses the following formula to generate the gain:

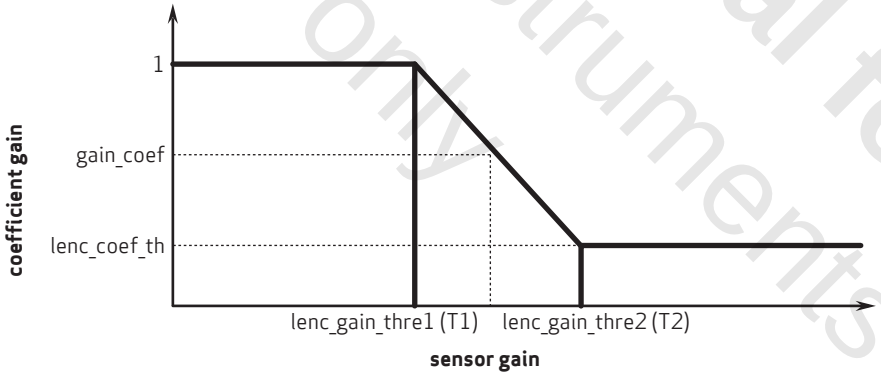
gain=a*r*r+b*r+1

where a and b is set by registers 0x3334~0x3337 for red, registers 0x333C~0x333F for green, and registers 0x3344~0x3347 for blue. R is the distance to the center of the image (center of the lens), that is, radius. "Gain" for center pixel is 1 (the minimum). "Gain" for perimeter pixels has a maximum of 5.

The parameters a and b also can be adjusted by the sensor gain.

The relationship of calculating the coefficient gain is shown in **figure 4-12**.

figure 4-12 coefficient gain graph



LENC control point parameters must be calibrated with a specific tool. Please contact your regional OmniVision FAE for assistance.

All LENC control registers are not frame-synced, thus any setting change will take effect immediately (during the current frame(N)).

table 4-2 LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x30A0	CROP_H_ST_H	0x00	RW	Start Address Horizontal High Byte
0x30A1	CROP_H_ST_L	0x00	RW	Start Address Horizontal Low Byte
0x30A2	CROP_V_ST_H	0x00	RW	Start Address Vertical High Byte
0x30A3	CROP_V_ST_L	0x00	RW	Start Address Vertical Low Byte
0x30A4	CROP_H_END_H	0x05	RW	End Address Horizontal High Byte
0x30A5	CROP_H_END_L	0x7F	RW	End Address Horizontal Low Byte
0x30A6	CROP_V_END_H	0x03	RW	End Address Vertical High Byte
0x30A7	CROP_V_END_L	0xDF	RW	End Address Vertical Low Byte
0x3250	ISP_DP_CONF1	0x33	RW	Bit[3]: lenc_en Enable lens correction
0x3330	LENC_RED_X0_H	0x02	RW	Red Center Horizontal Position (X0) High Byte
0x3331	LENC_RED_X0_L	0xC0	RW	Red Center Horizontal Position (X0) Low Byte
0x3332	LENC_RED_Y0_H	0x01	RW	Red Center Vertical Position (Y0) High Byte
0x3333	LENC_RED_Y0_L	0xF0	RW	Red Center Vertical Position (Y0) Low Byte
0x3334	LENC_RED_A1	0x00	RW	Red Parameter A1
0x3335	LENC_RED_A2	0x00	RW	Red Parameter A2
0x3336	LENC_RED_B1	0x00	RW	Red Parameter B1
0x3337	LENC_RED_B2	0x00	RW	Red Parameter B2
0x3338	LENC_GRN_X0_H	0x02	RW	Green Center Horizontal Position (X0) High Byte
0x3339	LENC_GRN_X0_L	0xC0	RW	Green Center Horizontal Position (X0) Low Byte
0x333A	LENC_GRN_Y0_H	0x01	RW	Green Center Vertical Position (Y0) High Byte
0x333B	LENC_GRN_Y0_L	0xF0	RW	Green Center Vertical Position (Y0) Low Byte
0x333C	LENC_GRN_A1	0x00	RW	Green Parameter A1
0x333D	LENC_GRN_A2	0x00	RW	Green Parameter A2
0x333E	LENC_GRN_B1	0x00	RW	Green Parameter B1
0x333F	LENC_GRN_B2	0x00	RW	Green Parameter B2
0x3340	LENC_BLU_X0_H	0x02	RW	Blue Center Horizontal Position (X0) High Byte
0x3341	LENC_BLU_X0_L	0xC0	RW	Blue Center Horizontal Position (X0) Low Byte
0x3342	LENC_BLU_Y0_H	0x01	RW	Blue Center Vertical Position (Y0) High Byte
0x3343	LENC_BLU_Y0_L	0xF0	RW	Blue Center Vertical Position (Y0) Low Byte

table 4-2 LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3344	LENC_BLU_A1	0x00	RW	Blue Parameter A1
0x3345	LENC_BLU_A2	0x00	RW	Blue Parameter A2
0x3346	LENC_BLU_B1	0x00	RW	Blue Parameter B1
0x3347	LENC_BLU_B2	0x00	RW	Blue Parameter B2
0x3348	LENC_CTRL	0x40	RW	Bit[7]: Not used Bit[6]: lenc_bias_plus Add bias back after LENC Bit[5:4]: real_gain_sel Select real gain to use for coefficient adjustment 00: HCG 01: LCG 10: VS 11: Not used Bit[3]: coef_man_en Override LENC gain coefficient with lenc_coef_man Bit[2]: gcoef_en Enables gain coefficient adjustment Bit[1]: quad_acc_en Bit[0]: rnd_en Adds random bits
0x3349	LENC_COEF_TH	0x00	RW	Coefficient Threshold (Minimum Level of Coefficient Gain) Format: 1.7, Max: 1.0
0x334A	LENC_GAIN_THRE1_H	0x00	RW	ISP Real Gain Threshold Low (No Sub-LSB) High Byte
0x334B	LENC_GAIN_THRE1_L	0x00	RW	ISP Real Gain Threshold Low (No Sub-LSB) Low Byte
0x334C	LENC_GAIN_THRE2_H	0x00	RW	ISP Real Gain Threshold High (No Sub-LSB) High Byte
0x334D	LENC_GAIN_THRE2_L	0x00	RW	ISP Real Gain Threshold High (No Sub-LSB) Low Byte
0x334E	LENC_COEF_MAN	0x80	RW	Manual Coefficient Scaling Parameter Format: 1.7, Max: 1.0

4.3 white balance gain (WB gain)

The next process in the pipeline is white balance. The RAW red, green and blue values of a gray object vary with the light source spectrum and the pixel QE spectrum response. Light source spectrum is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, the light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is about 2850K, while the color temperature of an overcast day is about 6500K.

To make sure that a gray image is truly gray regardless of the light spectrum, the sensor needs to adjust the gain for each RGB channel according to color temperature. This process is called white balance (WB).

The OV9716 WB gain registers can be controlled by a separate ISP processor.

The offset must be set by the registers 0x3378~0x339B for each capture channel and color channel. The offset value is calculated as:

offset = (WB_gain - 1) × blc_target

White balance gain is enabled/disabled in register 0x3250[1]. The applied WB gain can be read back from registers 0x3360~0x3377 and offset values can be read back from registers 0x3378~0x339B.

All WB control registers are not frame-synced, thus any setting change will take effect immediately (during the current frame(N).

table 4-3 WB control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3250	ISP_DP_CONF1	0x33	RW	Bit[1]: wb_gain_en WB_gain enable
0x3360	R_GAIN_HCG_H	0x01	RW	Gain for HCG Channel Red Component High Byte
0x3361	R_GAIN_HCG_L	0x00	RW	Gain for HCG Channel Red Component Low Byte
0x3362	GR_GAIN_HCG_H	0x01	RW	Gain for HCG Channel Greenr Component High Byte
0x3363	GR_GAIN_HCG_L	0x00	RW	Gain for HCG Channel Greenr Component Low Byte
0x3364	GB_GAIN_HCG_H	0x01	RW	Gain for HCG Channel Greenb Component High Byte
0x3365	GB_GAIN_HCG_L	0x00	RW	Gain for HCG Channel Greenb Component Low Byte
0x3366	B_GAIN_HCG_H	0x01	RW	Gain for HCG Channel Blue Component High Byte
0x3367	B_GAIN_HCG_L	0x00	RW	Gain for HCG Channel Blue Component Low Byte
0x3368	R_GAIN_LCG_H	0x01	RW	Gain for LCG Channel Red Component High Byte
0x3369	R_GAIN_LCG_L	0x00	RW	Gain for LCG Channel Red Component Low Byte
0x336A	GR_GAIN_LCG_H	0x01	RW	Gain for LCG Channel Greenr Component High Byte
0x336B	GR_GAIN_LCG_L	0x00	RW	Gain for LCG Channel Greenr Component Low Byte

table 4-3 WB control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x336C	GB_GAIN_LCG_H	0x01	RW	Gain for LCG Channel Greenb Component High Byte
0x336D	GB_GAIN_LCG_L	0x00	RW	Gain for LCG Channel Greenb Component Low Byte
0x336E	B_GAIN_LCG_H	0x01	RW	Gain for LCG Channel Blue Component High Byte
0x336F	B_GAIN_LCG_L	0x00	RW	Gain for LCG Channel Blue Component Low Byte
0x3370	R_GAIN_VS_H	0x01	RW	Gain for VS Channel Red Component High Byte
0x3371	R_GAIN_VS_L	0x00	RW	Gain for VS Channel Red Component Low Byte
0x3372	GR_GAIN_VS_H	0x01	RW	Gain for VS Channel Greenr Component High Byte
0x3373	GR_GAIN_VS_L	0x00	RW	Gain for VS Channel Greenr Component Low Byte
0x3374	GB_GAIN_VS_H	0x01	RW	Gain for VS Channel Greenb Component High Byte
0x3375	GB_GAIN_VS_L	0x00	RW	Gain for VS Channel Greenb Component Low Byte
0x3376	B_GAIN_VS_H	0x01	RW	Gain for VS Channel Blue Component High byte
0x3377	B_GAIN_VS_L	0x00	RW	Gain for VS Channel Blue Component Low byte
0x3378	R_OFFSET_HCG_H	0x00	RW	Offset for HCG Channel Red Component High Byte
0x3379	R_OFFSET_HCG_M	0x00	RW	Offset for HCG Channel Red Component Middle Byte
0x337A	R_OFFSET_HCG_L	0x00	RW	Offset for HCG Channel Red Component Low Byte
0x337B	GR_OFFSET_HCG_H	0x00	RW	Offset for HCG Channel Greenr Component High Byte
0x337C	GR_OFFSET_HCG_M	0x00	RW	Offset for HCG Channel Greenr Component Middle Byte
0x337D	GR_OFFSET_HCG_L	0x00	RW	Offset for HCG Channel Greenr Component Low Byte
0x337E	GB_OFFSET_HCG_H	0x00	RW	Offset for HCG Channel Greenb Component High Byte
0x337F	GB_OFFSET_HCG_M	0x00	RW	Offset for HCG Channel Greenb Component Middle Byte
0x3380	GB_OFFSET_HCG_L	0x00	RW	Offset for HCG Channel Greenb Component Low Byte
0x3381	B_OFFSET_HCG_H	0x00	RW	Offset for HCG Channel Blue Component High Byte
0x3382	B_OFFSET_HCG_M	0x00	RW	Offset for HCG Channel Blue Component Middle Byte
0x3383	B_OFFSET_HCG_L	0x00	RW	Offset for HCG Channel Blue Component Low Byte
0x3384	R_OFFSET_LCG_H	0x00	RW	Offset for LCG Channel Red Component High Byte
0x3385	R_OFFSET_LCG_M	0x00	RW	Offset for LCG Channel Red Component Middle Byte

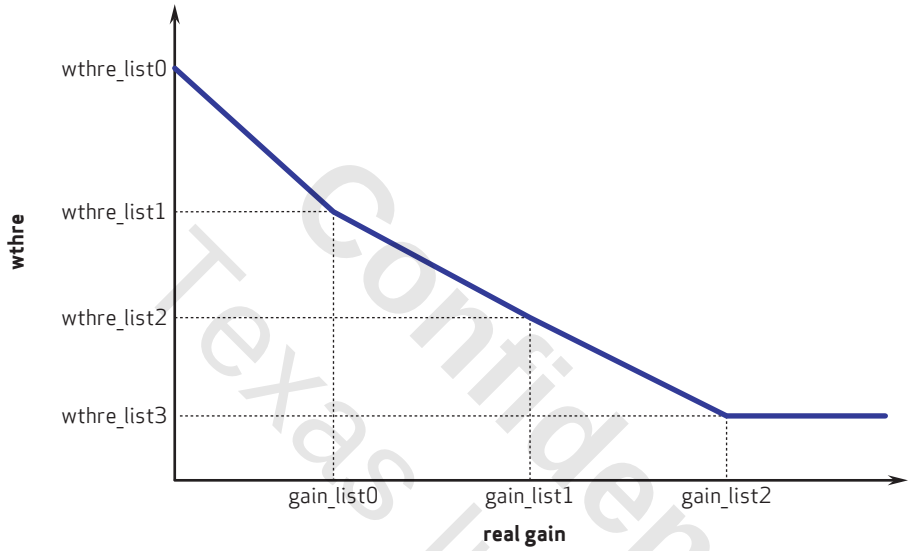
table 4-3 WB control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3386	R_OFFSET_LCG_L	0x00	RW	Offset for LCG Channel Red Component Low Byte
0x3387	GR_OFFSET_LCG_H	0x00	RW	Offset for LCG Channel Greenr Component High Byte
0x3388	GR_OFFSET_LCG_M	0x00	RW	Offset for LCG Channel Greenr Component Middle Byte
0x3389	GR_OFFSET_LCG_L	0x00	RW	Offset for LCG Channel Greenr Component Low Byte
0x338A	GB_OFFSET_LCG_H	0x00	RW	Offset for LCG Channel Greenb Component High Byte
0x338B	GB_OFFSET_LCG_M	0x00	RW	Offset for LCG Channel Greenb Component Middle Byte
0x338C	GB_OFFSET_LCG_L	0x00	RW	Offset for LCG Channel Greenb Component Low Byte
0x338D	B_OFFSET_LCG_H	0x00	RW	Offset for LCG Channel Blue Component High Byte
0x338E	B_OFFSET_LCG_M	0x00	RW	Offset for LCG Channel Blue Component Middle byte
0x338F	B_OFFSET_LCG_L	0x00	RW	Offset for LCG Channel Blue Component Low Byte
0x3390	R_OFFSET_VS_H	0x00	RW	Offset for VS Channel Red Component High Byte
0x3391	R_OFFSET_VS_M	0x00	RW	Offset for VS Channel Red Component Middle Byte
0x3392	R_OFFSET_VS_L	0x00	RW	Offset for VS Channel Red Component Low Byte
0x3393	GR_OFFSET_VS_H	0x00	RW	Offset for VS Channel Greenr Component High Byte
0x3394	GR_OFFSET_VS_M	0x00	RW	Offset for VS Channel Greenr Component Middle Byte
0x3395	GR_OFFSET_VS_L	0x00	RW	Offset for VS Channel Greenr Component Low Byte
0x3396	GB_OFFSET_VS_H	0x00	RW	Offset for VS Channel Greenb Component High Byte
0x3397	GB_OFFSET_VS_M	0x00	RW	Offset for VS Channel Greenb Component Middle Byte
0x3398	GB_OFFSET_VS_L	0x00	RW	Offset for VS Channel Greenb Component Low Byte
0x3399	B_OFFSET_VS_H	0x00	RW	Offset for VS Channel Blue Component High Byte
0x339A	B_OFFSET_VS_M	0x00	RW	Offset for VS Channel Blue Component Middle Byte
0x339B	B_OFFSET_VS_L	0x00	RW	Offset for VS Channel Blue Component Low Byte

4.4 defective pixel cancellation (DPC)

The DPC function detects defect pixels/clusters by using a programmable threshold. The threshold can be set manually by registers or automatically calculated based on analog gain. Refer to figure **figure 4-13** for details.

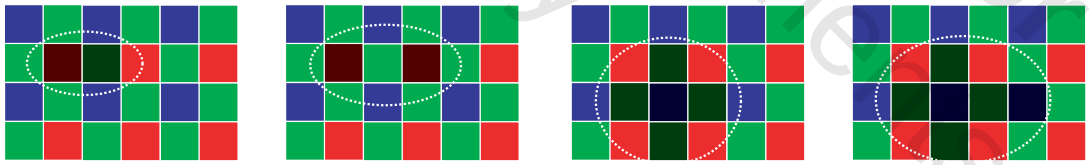
figure 4-13 threshold gain curve



note Bthre = Wthre * (8+thre_ratio)/8

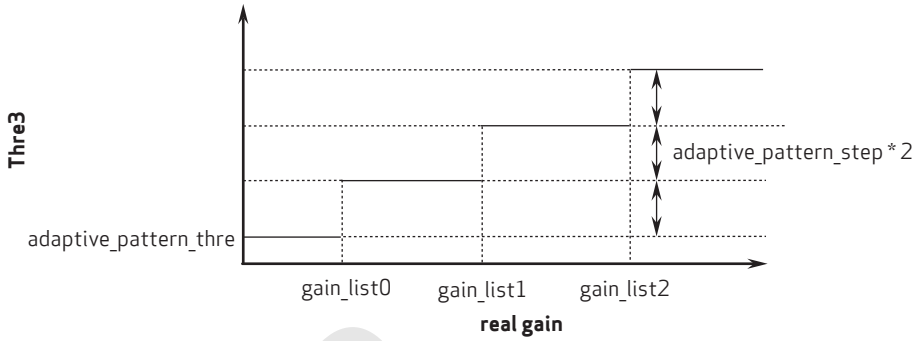
The DPC can correct single defect pixel, couplet, cross type and tail type cluster (refer to **table 4-4** for the enable/disable controls for each type of defect). **figure 4-14** shows the sample defect pattern of couplet, cross and tail cluster defect.

figure 4-14 defect pattern examples



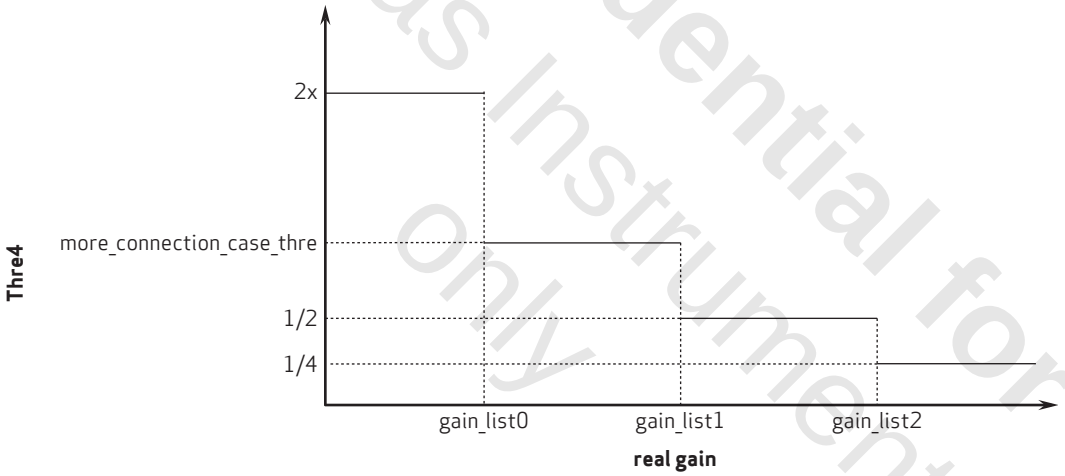
different color plane couplet | same color plane couplet | cross type cluster | tail type cluster

figure 4-15 adaptive thresholds



If there are two similar defective pixels not far from each other, they cannot be recovered. To resolve this, the DPC algorithm will only search for similar patterns in high frequency regions. When the difference between minimum and maximum values are below the adaptive threshold, the current pixel is considered located in a high frequency region. Smaller threshold values will retain more image details.

figure 4-16 connected case thresholds



When detecting the same or different channel connected defect pixels, the difference between the central pixel and surrounding normal pixels must be below this threshold. Compared to a single white or black pixel, these clusters will further degrade the image quality, thus a separate threshold is designed for them. These thresholds are higher than single defect pixel thresholds as connected cases are less common.

table 4-4 DPC registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x33E0	CTRL_DPC_00_VS	0x14	RW	DPC Control 0, VS Bit[5]: enable_tail Tail enable, enable_crosscluster must also be set Bit[4]: enable_saturate_crosscluster Saturate cross-cluster enable, enable_crosscluster must also be set Bit[3]: enable_3x3_cluster 3x3 cluster enable Bit[2]: enable_crosscluster Cross-cluster enable Bit[1]: enable_general_tail General tail enable, three horizontal connected clusters with one of pixels exceeding saturation value Bit[0]: manual_mode_en Manual mode enable
0x33E1	CTRL_DPC_01_VS	0x0F	RW	DPC Control 1, VS Bit[7:4]: Saturate Saturate pixel saturation threshold Bit[3]: enable_diffchannel_wpconn Different channel white pixel correction enable Bit[2]: enable_diffchannel_bpconn Different channel black pixel correction enable Bit[1]: enable_samechannel_wpconn Same channel white pixel correction enable Bit[0]: enable_samechannel_bpconn Same channel black pixel correction enable
0x33E2	CTRL_DPC_02_VS	0x04	RW	White Threshold List0, VS
0x33E3	CTRL_DPC_03_VS	0x02	RW	White Threshold List1, VS
0x33E4	CTRL_DPC_04_VS	0x01	RW	White Threshold List2, VS
0x33E5	CTRL_DPC_05_VS	0x01	RW	White Threshold List3, VS
0x33E6	CTRL_DPC_06_VS	0x00	RW	Adaptive Pattern Thresholds, VS
0x33E7	CTRL_DPC_07_VS	0x04	RW	Adaptive Pattern Step, VS
0x33E8	CTRL_DPC_08_VS	0x0C	RW	More Connection Case Thresholds, VS
0x33E9	CTRL_DPC_09_VS	0x00	RW	DPC Level List0, VS DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality worsens.

table 4-4 DPC registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x33EA	CTRL_DPC_10_VS	0x01	RW	DPC Level List1, VS
0x33EB	CTRL_DPC_11_VS	0x02	RW	DPC Level List2, VS
0x33EC	CTRL_DPC_12_VS	0x03	RW	DPC Level List3, VS
0x33ED	CTRL_DPC_13_VS	0x03	RW	Gain List0, VS
0x33EE	CTRL_DPC_14_VS	0x0F	RW	Gain List1, VS
0x33EF	CTRL_DPC_15_VS	0x3F	RW	Gain List2, VS
0x33F0	CTRL_DPC_16_VS	0x08	RW	Matching Thresholds, VS If a similar pattern in neighbor of central defect pixel is found, this value will be used to determine similarity between pixels. If difference between two pixels is larger than this threshold, two are not considered similar. larger threshold will maintain more image detail.
0x33F1	CTRL_DPC_17_VS	0x04	RW	Status Thresholds, VS A pixel is marked as defective if original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x33F2	CTRL_DPC_18_VS	0x04	RW	Threshold Ratio, VS Ratio of white threshold and black threshold
0x33F3	CTRL_DPC_19_VS	0x00	RW	Clip Interpolate G Enable, VS Controls whether or not to remove defective pixels in B or R channel when G channel is saturated
0x33F4	CTRL_DPC_20_VS	0x03	RW	Edge Option, VS Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate adjacent same channel data for padding 11: Duplicate upper same channel data for padding

table 4-4 DPC registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x33F5	CTRL_DPC_00_L	0x14	RW	DPC Control 0, HCG Bit[5]: enable_tail Tail enable, enable_crosscluster must also be set Bit[4]: enable_saturate_crosscluster Saturate cross-cluster enable, enable_crosscluster must also be set Bit[3]: enable_3x3_cluster 3x3 cluster enable Bit[2]: enable_crosscluster Cross-cluster enable Bit[1]: enable_general_tail General tail enable, three horizontal connected clusters with one of pixels exceeding saturation value Bit[0]: manual_mode_en Manual mode enable
0x33F6	CTRL_DPC_01_L	0x0F	RW	DPC Control 1, HCG Bit[7:4]: Saturate pixel saturation threshold Bit[3]: enable_diffchannel_wpconn Different channel white pixel correction enable Bit[2]: enable_diffchannel_bpconn Different channel black pixel correction enable Bit[1]: enable_samechannel_wpconn Same channel white pixel correction enable Bit[0]: enable_samechannel_bpconn Same channel black pixel correction enable
0x33F7	CTRL_DPC_02_L	0x04	RW	White Threshold List0, HCG
0x33F8	CTRL_DPC_03_L	0x02	RW	White Threshold List1, HCG
0x33F9	CTRL_DPC_04_L	0x01	RW	White Threshold List2, HCG
0x33FA	CTRL_DPC_05_L	0x01	RW	White Threshold List3, HCG
0x33FB	CTRL_DPC_06_L	0x00	RW	Adaptive Pattern Thresholds, HCG
0x33FC	CTRL_DPC_07_L	0x04	RW	Adaptive Pattern Step, HCG
0x33FD	CTRL_DPC_08_L	0x0C	RW	More Connection Case Thresholds, HCG
0x33FE	CTRL_DPC_09_L	0x00	RW	DPC Level List0, HCG DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality worsens.
0x33FF	CTRL_DPC_10_L	0x01	RW	DPC Level List1, HCG

table 4-4 DPC registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x3400	CTRL_DPC_11_L	0x02	RW	DPC Level List2, HCG
0x3401	CTRL_DPC_12_L	0x03	RW	DPC Level List3, HCG
0x3402	CTRL_DPC_13_L	0x03	RW	Gain List0, HCG
0x3403	CTRL_DPC_14_L	0x0F	RW	Gain List1, HCG
0x3404	CTRL_DPC_15_L	0x3F	RW	Gain List2, HCG
0x3405	CTRL_DPC_16_L	0x08	RW	Matching Thresholds, HCG If a similar pattern in neighbor of central defect pixel is found, this value will be used to determine similarity between pixels. If difference between two pixels is larger than this threshold, two are not considered similar. larger threshold will maintain more image detail.
0x3406	CTRL_DPC_17_L	0x04	RW	Status Thresholds, HCG A pixel is marked as defective if original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x3407	CTRL_DPC_18_L	0x04	RW	Threshold Ratio, HCG Ratio of white threshold and black threshold
0x3408	CTRL_DPC_19_L	0x00	RW	Clip Interpolate G Enable, HCG Controls whether or not to remove defective pixels in B or R channel when G channel is saturated
0x3409	CTRL_DPC_20_L	0x03	RW	Edge Option, HCG Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate adjacent same channel data for padding 11: Duplicate upper same channel data for padding

table 4-4 DPC registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x340A	CTRL_DPC_00_S	0x14	RW	DPC Control 0, LCG Bit[5]: enable_tail Tail enable, enable_crosscluster must also be set Bit[4]: enable_saturate_crosscluster Saturate cross-cluster enable, enable_crosscluster must also be set Bit[3]: enable_3x3_cluster 3x3 cluster enable Bit[2]: enable_crosscluster Cross-cluster enable Bit[1]: enable_general_tail General tail enable, three horizontal connected clusters with one of pixels exceeding saturation value Bit[0]: manual_mode_en Manual mode enable
0x340B	CTRL_DPC_01_S	0x0F	RW	DPC Control 1, LCG Bit[7:4]: Saturate Saturate pixel saturation threshold Bit[3]: enable_diffchannel_wpconn Different channel white pixel correction enable Bit[2]: enable_diffchannel_bpconn Different channel black pixel correction enable Bit[1]: enable_samechannel_wpconn Same channel white pixel correction enable Bit[0]: enable_samechannel_bpconn Same channel black pixel correction enable
0x340C	CTRL_DPC_02_S	0x04	RW	White Threshold List0, LCG
0x340D	CTRL_DPC_03_S	0x02	RW	White Threshold List1, LCG
0x340E	CTRL_DPC_04_S	0x01	RW	White Threshold List2, LCG
0x340F	CTRL_DPC_05_S	0x01	RW	White Threshold List3, LCG
0x3410	CTRL_DPC_06_S	0x00	RW	Adaptive Pattern Thresholds, LCG
0x3411	CTRL_DPC_07_S	0x04	RW	Adaptive Pattern Step, LCG
0x3412	CTRL_DPC_08_S	0x0C	RW	More Connection Case Thresholds, LCG
0x3413	CTRL_DPC_09_S	0x00	RW	DPC Level List0, LCG DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality worsens.

table 4-4 DPC registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x3414	CTRL_DPC_10_S	0x01	RW	DPC Level List1, LCG
0x3415	CTRL_DPC_11_S	0x02	RW	DPC Level List2, LCG
0x3416	CTRL_DPC_12_S	0x03	RW	DPC Level List3, LCG
0x3417	CTRL_DPC_13_S	0x03	RW	Gain List0, LCG
0x3418	CTRL_DPC_14_S	0x0F	RW	Gain List1, LCG
0x3419	CTRL_DPC_15_S	0x3F	RW	Gain List2, LCG
0x341A	CTRL_DPC_16_S	0x08	RW	Matching Thresholds, LCG If a similar pattern in neighbor of central defect pixel is found, this value will be used to determine similarity between pixels. If difference between two pixels is larger than this threshold, two are not considered similar. larger threshold will maintain more image detail.
0x341B	CTRL_DPC_17_S	0x04	RW	Status Thresholds, LCG A pixel is marked as defective if original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x341C	CTRL_DPC_18_S	0x04	RW	Threshold Ratio, LCG Ratio of White Threshold and Black Threshold
0x341D	CTRL_DPC_19_S	0x00	RW	Clip Interpolate G enable, LCG Controls Whether or Not to Remove Defective Pixels in B or R Channel When G Channel is Saturated
0x341E	CTRL_DPC_20_S	0x03	RW	Edge Option, LCG Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate adjacent same channel data for padding 11: Duplicate upper same channel data for padding
0x341F	CTRL_DPC_21_VS	–	R	Black Threshold, VS
0x3420	CTRL_DPC_22_VS	–	R	White Threshold, VS
0x3421	CTRL_DPC_23_VS	–	R	Threshold 1, VS
0x3422	CTRL_DPC_24_VS	–	R	Threshold 2, VS
0x3423	CTRL_DPC_25_VS	–	R	Threshold 3, VS
0x3424	CTRL_DPC_26_VS	–	R	Threshold 4, VS
0x3425	CTRL_DPC_27_VS	–	R	Level, VS

table 4-4 DPC registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x3426	CTRL_DPC_21_L	–	R	Black Threshold, HCG
0x3427	CTRL_DPC_22_L	–	R	White Threshold, HCG
0x3428	CTRL_DPC_23_L	–	R	Threshold 1, HCG
0x3429	CTRL_DPC_24_L	–	R	Threshold 1, HCG
0x342A	CTRL_DPC_25_L	–	R	Threshold 1, HCG
0x342B	CTRL_DPC_26_L	–	R	Threshold 1, HCG
0x342C	CTRL_DPC_27_L	–	R	Level, HCG
0x342D	CTRL_DPC_21_S	–	R	Black Threshold, LCG
0x342E	CTRL_DPC_22_S	–	R	White Threshold, LCG
0x342F	CTRL_DPC_23_S	–	R	Threshold 1, LCG
0x3430	CTRL_DPC_24_S	–	R	Threshold 1, LCG
0x3431	CTRL_DPC_25_S	–	R	Threshold 1, LCG
0x3432	CTRL_DPC_26_S	–	R	Threshold 1, LCG
0x3433	CTRL_DPC_27_S	–	R	Level, LCG

4.5 HDR combine principle

figure 4-17 shows the principle of HDR combine.

- For linear mode, output data is 12 bit linear data.
- For single exposure HDR mode, data output can be 16-bit linear data or both 12-bit HCG and LCG data. User can combine HCG and LCG into 16 bit HDR data. Ratio between HCG and LCG is determined by conversion gain, analog gain, and digital gain. This ratio should not exceed 16. For example, if conversion gain is 10, (HCG_analog_gain x HCG_digital_gain)/(LCG_analog_gain x LCG_digital_gain) should not be greater than 1.6.
- HCG/LCG analog gain ratio cannot exceed 2 due to the algorithm limitation.
- In order to get 20 bit image data, dual exposure mode should be used. Ratio between LCG and VS is determined by exposure time and gain

figure 4-17 HDR combine principle diagram

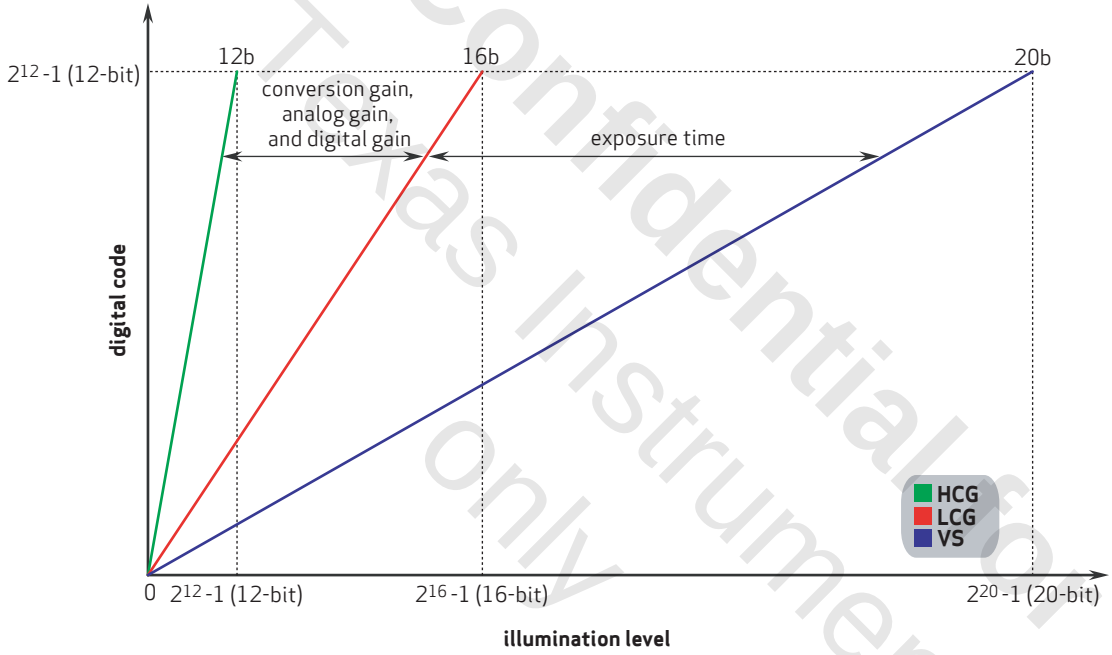


table 4-5 combine control register

address	register name	default value	R/W	description
0x3250	ISP_DP_CONF1	0x33	RW	Bit[4]: comb_en DCG combine enable

5 image output interface

5.1 image output format

table 5-1 summarizes the output formats which the OV9716 supports.

table 5-1 image output format summary

format		description
linear	12b	12-bit RAW data, either HCG or LCG
dual exposure HDR	16b DCG + 12b VS	{16-bit combined DCG data} + {12-bit RAW VS}
	12b compressed DCG + 12b VS	{12-bit data compressed from 16-bit DCG combined data} + {(12-bit RAW VS)}
	3x12b	{12-bit HCG} + {12-bit LCG} + {12-bit RAW VS}
	3x10b compressed	compressed from 3x12b DCG
	12b RAW (HCG or LCG) + 12b VS	{12-bit HCG or LCG} + {12-bit RAW VS}
single exposure HDR	16b DCG	16-bit combined DCG data
	12b compressed DCG	12-bit data compressed from 16-bit combined DCG data
	2x12b	{12-bit HCG} + {12-bit LCG}

Register interface_control0 with address 0x3190[7:0] is used for interface control.

table 5-2 interface control register

address	register name	default value	R/W	description
0x3190	INTERFACE_CTRL0	0x07	RW	Bit[7]: channel_cfg Channel configuration Bit[6]: Linear mode conversion gain 0: LCG 1: HCG Bit[5]: mode_10b Output 10-bit data, only supported by some modes Bit[4]: no_comp When high, single 12 bits data are sent without compression Bit[3]: lin_enable Fast linear mode enable (not supported, logic is kept, but not verified) Bit[2]: vs_enable Staggered VS mode enable Bit[1:0]: data_width 00: Not used 01: 2x12 10: 12 combined 11: 16 combined

table 5-3 represents the interface_ctrl0 setting for different output formats.

table 5-3 register setting for different output formats

format		register setting[a]					
		0x3190[7] chanel_cfg	0x3190[6] format_sel	0x3190[5] 10b_mode	0x3190[3] lin_enable	0x3190[2] vs_enable	0x3190[1:0] data_width
linear	12b	1	0 (LCG), 1 (HCG)	0	0	0	01
dual exposure HDR	16b DCG + 12b VS	x	x	x	0	1	11
	12b compressed DCG + 12b VS	x	x	x	0	1	10
	3x12b	0	x	0	0	1	01
	3x10b compressed	0	x	1	0	1	01
	12b RAW (HCG or LCG) + 12b VS	1	0: LCG 1: HCG	0	0	1	01
single exposure HDR	16b DCG	x	x	x	0	0	11
	12b compressed DCG	x	x	x	0	0	10
	2x12b	0	x	x	0	0	01

a. x means do not care

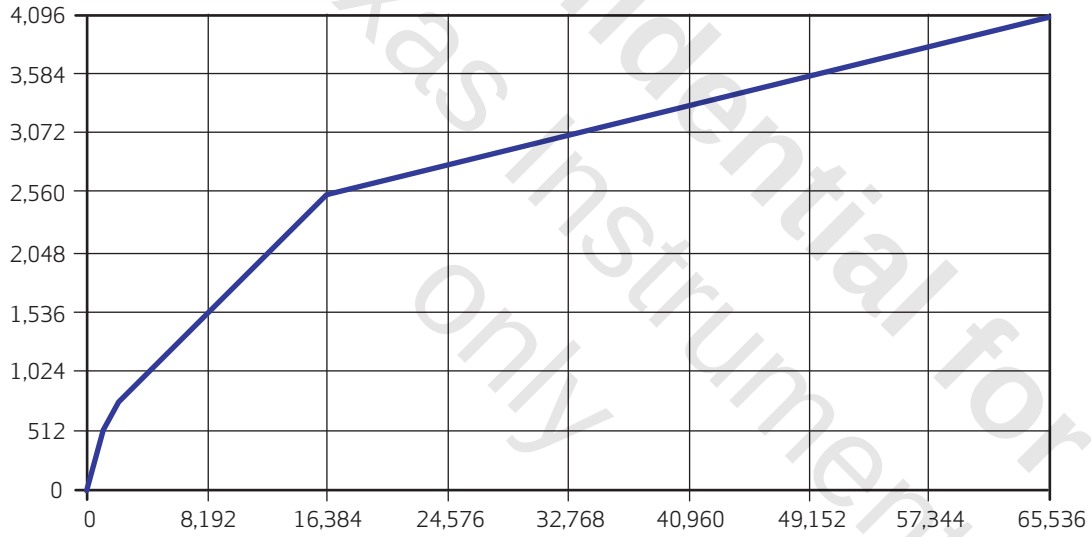
5.2 data compression algorithm

5.2.1 DCG 16b to compressed DCG 12b

The OV9716 has a data compression from DCG 16-bit to compressed DCG 12-bit by a 4-piece piece-wise linear (PWL) curve defined by the following formula and shown in **figure 5-1**.

$$y_{out\_12b} = \begin{cases} \frac{y_{in\_16b}}{2}, & y_{in\_16b} < 1024 \\ \frac{y_{in\_16b}}{4} + 256, & 1024 \le y_{in\_16b} < 2048 \\ \frac{y_{in\_16b}}{8} + 512, & 2048 \le y_{in\_16b} < 16384 \\ \frac{y_{in\_16b}}{32} + 2048, & y_{in\_16b} \ge 16384 \end{cases}$$

figure 5-1 16-bit to 12-bit PWL compression



The backend processor can decompress 12-bit data to 16-bit data using the following formula.

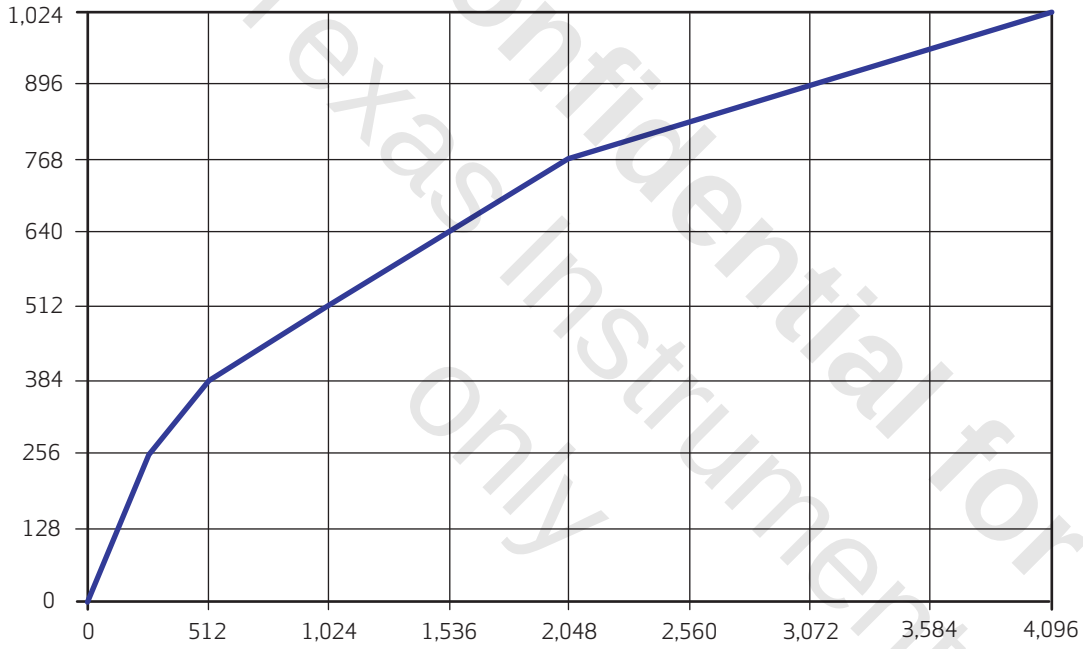
$$\mathbf{y_{out\_16b}} = \begin{cases} \mathbf{2 \times y_{in\_12b}}, & \mathbf{y_{in\_12b} < 512} \\ \mathbf{4 \times (y_{in\_12b} - 256)}, & \mathbf{512 \le y_{in\_12b} < 768} \\ \mathbf{8 \times (y_{in\_12b} - 512)}, & \mathbf{768 \le y_{in\_12b} < 2560} \\ \mathbf{32 \times (y_{in\_12b} - 2048)}, & \mathbf{y_{in\_12b} \ge 2560} \end{cases}$$

5.2.2 linear 12b to linear 10b

The OV9716 has a data compression from linear 12-bit to linear 10-bit by a 4-piece PWL curve defined by the following formula and as shown in **figure 5-2**.

$$y_{out\_10b} = \begin{cases} y_{in\_12b}, & y_{in\_12b} < 256 \\ \frac{y_{in\_12b}}{2} + 128, & 256 \le y_{in\_12b} < 512 \\ \frac{y_{in\_12b}}{4} + 256, & 512 \le y_{in\_12b} < 2048 \\ \frac{y_{in\_12b}}{8} + 512, & y_{in\_12b} \ge 2048 \end{cases}$$

figure 5-2 12-bit to 10-bit PWL compression



The backend processor can decompress 10-bit data to 12-bit data using the following formula.

$$y_{out\_12b} = \begin{cases} y_{in\_10b}, & y_{in\_10b} < 256 \\ 2 \times (y_{in\_10b} - 128), & 256 \le y_{in\_10b} < 384 \\ 4 \times (y_{in\_10b} - 256), & 384 \le y_{in\_10b} < 768 \\ 8 \times (y_{in\_10b} - 512), & y_{in\_10b} \ge 768 \end{cases}$$

5.3 HDR output

The OV9716 supports MIPI and DVP output interface, which will be described by the following sections.

In staggered HDR mode, HCG/LCG exposure frames are overlapping with VS exposures. This reduces the timing delay between different exposure frames, which will be combined into one HDR frame. It also reduces the frame/line buffer requirement for the backend chip.

5.3.1 MIPI

The MIPI interface supports 1, 2, or 4 lanes. The data output format is the same regardless of how many lanes are used with MIPI. The data packet illustrations in this section are to be interpreted line-wise as one consecutive data stream and show the layout of the data packet. The data packet is divided up between the lanes per byte (8 bits) according to MIPI CSI-2. MIPI global timing is set in registers 0x31E3 and 0x31E4

For non-staggered HDR, the OV9716 outputs multiple captures over different virtual channels or one single shared virtual channel, where each capture is output line-interleaved as shown in **figure 5-3** and **figure 5-4**. Short-packets denote frame-start (FS) and frame-end (FE) on the respective virtual channel. If only one capture is output from the sensor, virtual channel 0 is used as default.

For staggered HDR, the OV9716 outputs multiple captures over different virtual channels or one single shared virtual channel. In either case, the output of actual exposure data is staggered in the time axis, as shown in **figure 5-5** and **figure 5-6**, respectively. In shared virtual channel mode, only one FS and FE packet is sent out per frame, and dummy data will be sent in the absence of actual exposure data, as shown in **figure 5-6**. In non-shared virtual channel mode, FS and FE short packets denote the frame start and frame end of their respective virtual channel, and no dummy data is sent out.

The VS exposure plus HCG/LCG exposure should be less than vertical total size (VTS):

Max_exposure_VS + Max_exposure_HCG/LCG < VTS - 2

figure 5-3 non-staggered HDR with MIPI virtual channel diagram

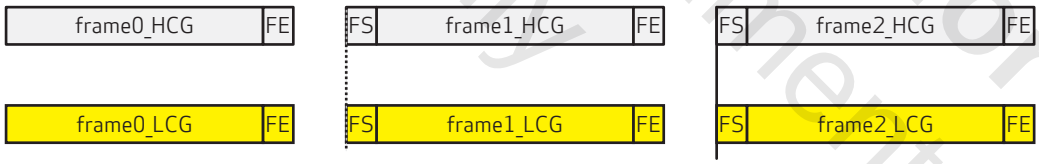


figure 5-4 non-staggered HDR with MIPI virtual channel detail diagram

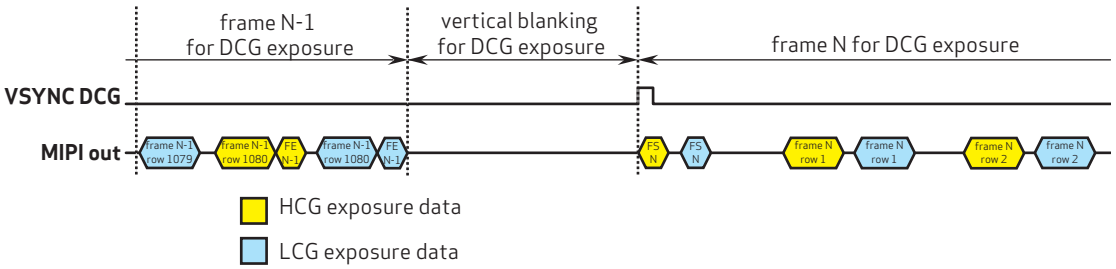


figure 5-5 staggered HDR with MIPI virtual channel diagram

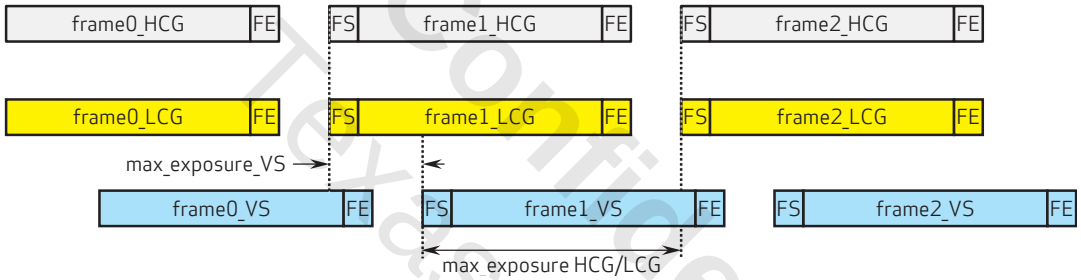


figure 5-6 staggered HDR with MIPI virtual channel detail diagram

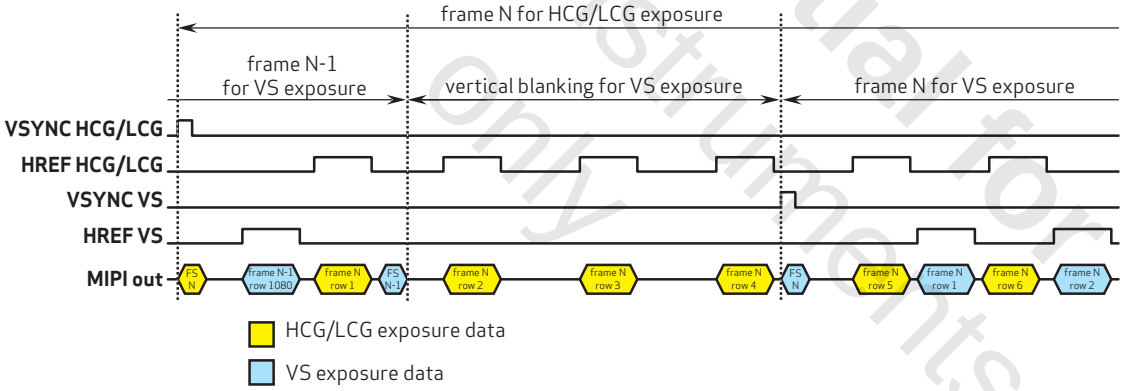


figure 5-7 non-staggered HDR without MIPI virtual channel overview diagram

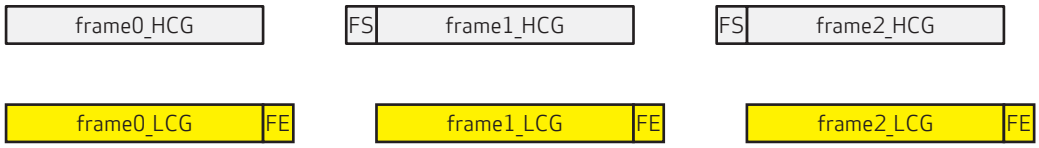


figure 5-8 non-staggered HDR without MIPI virtual channel detail diagram

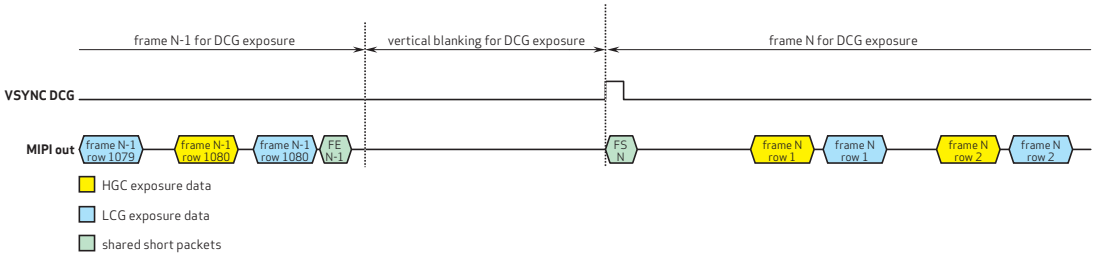


figure 5-9 staggered HDR without MIPI virtual channel overview diagram

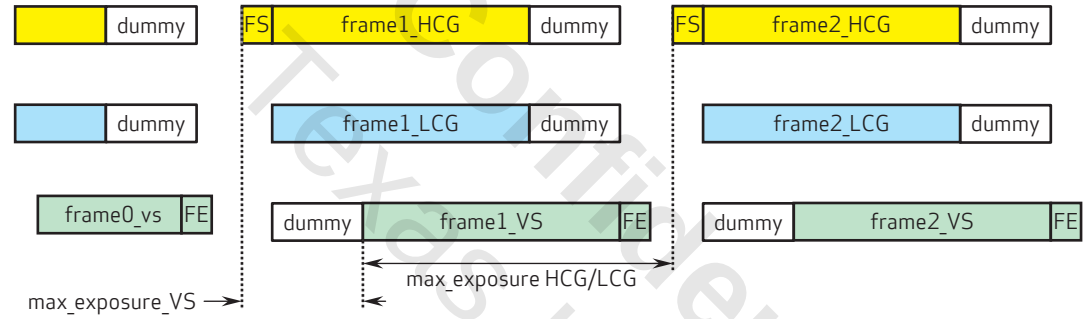


figure 5-10 staggered HDR without MIPI virtual channel detail diagram

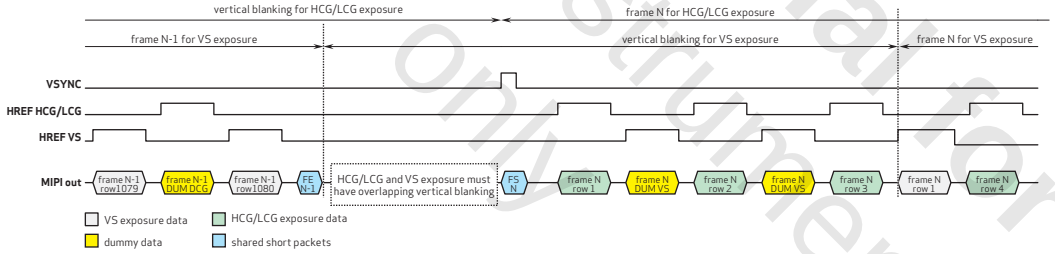


table 5-4 represents the resolution and maximum frame rate for MIPI with different output format.

table 5-4 supported output formats and frame rates for MIPI (sheet 1 of 2)

maximum frame rate supported via MIPI (960 Mbps/lane) interface at 1392x976		
format		maximum frame rate
linear	12b	60 fps

table 5-4 supported output formats and frame rates for MIPI (sheet 2 of 2)

maximum frame rate supported via MIPI (960 Mbps/lane) interface at 1392x976		
format		maximum frame rate
dual exposure HDR	16b DCG+12b VS	60 fps
	12b compressed DCG +12b VS	60 fps
	3x12b (3x10b)	60 fps (60 fps)
	12b RAW (HCG or LCG) + 12b VS	60 fps
single exposure HDR	16b DCG	60 fps
	12b compressed DCG	60 fps
	2x12b	60 fps

table 5-5 defines the default MIPI RAW image data type codes. The values are defined by the register listed in **table 5-5**.

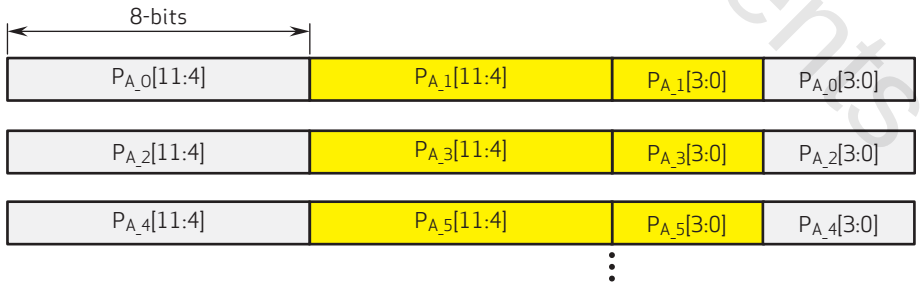
table 5-5 MIPI RAW image data types

default data type	register address	description
2B	0x3211	RAW 10
2C	0x3210	RAW 12
30	0x320E	RAW 16

5.3.1.1 12b linear mode

One value per pixel: P_A (12-bit RAW)

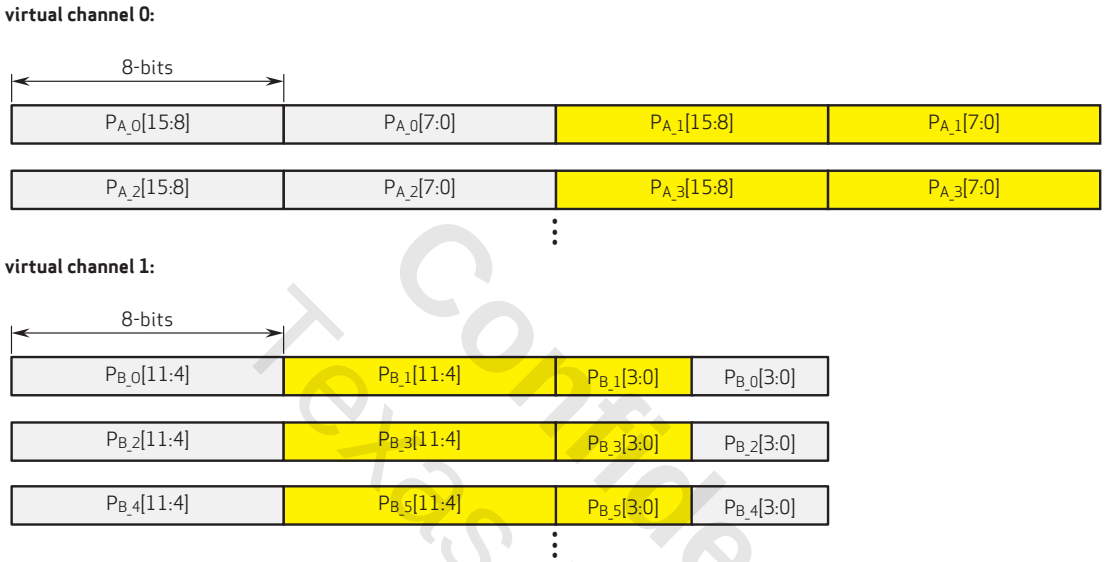
figure 5-11 12b linear mode diagram



5.3.1.2 16b DCG + 12b VS dual HDR

Two values per pixel: P_A (16-bit combined DCG), P_B (12-bit RAW)

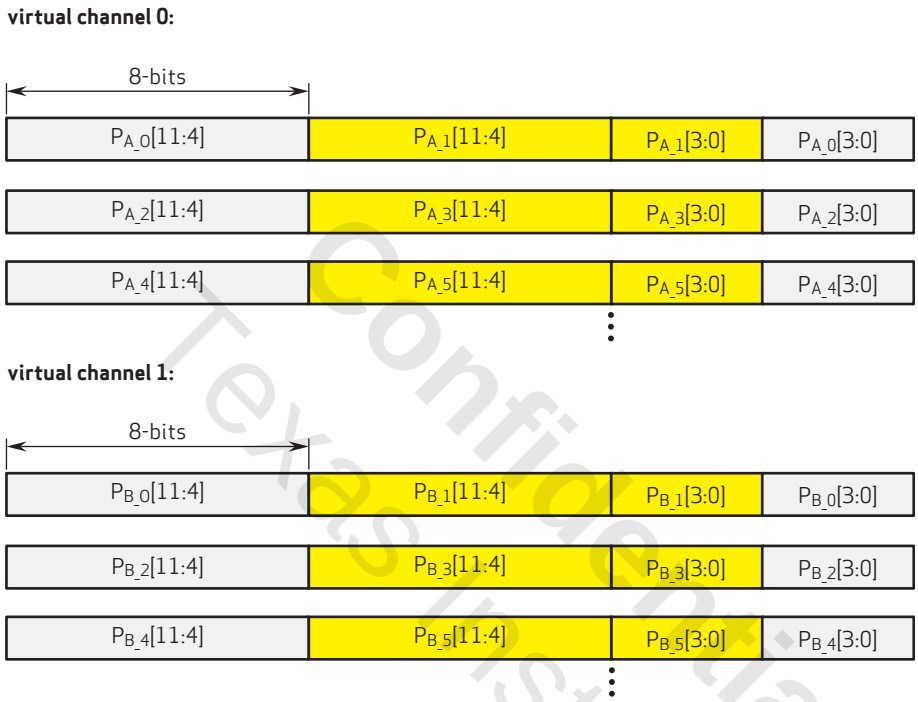
figure 5-12 16b DCG + 12b VS dual HDR diagram



5.3.1.3 12b compressed DCG + 12b VS dual HDR

Two values per pixel: P_A (12-bit, compressed from 16-bit combined DCG), P_B (12-bit RAW)

figure 5-13 12b compressed DCG + 12b VS dual HDR diagram

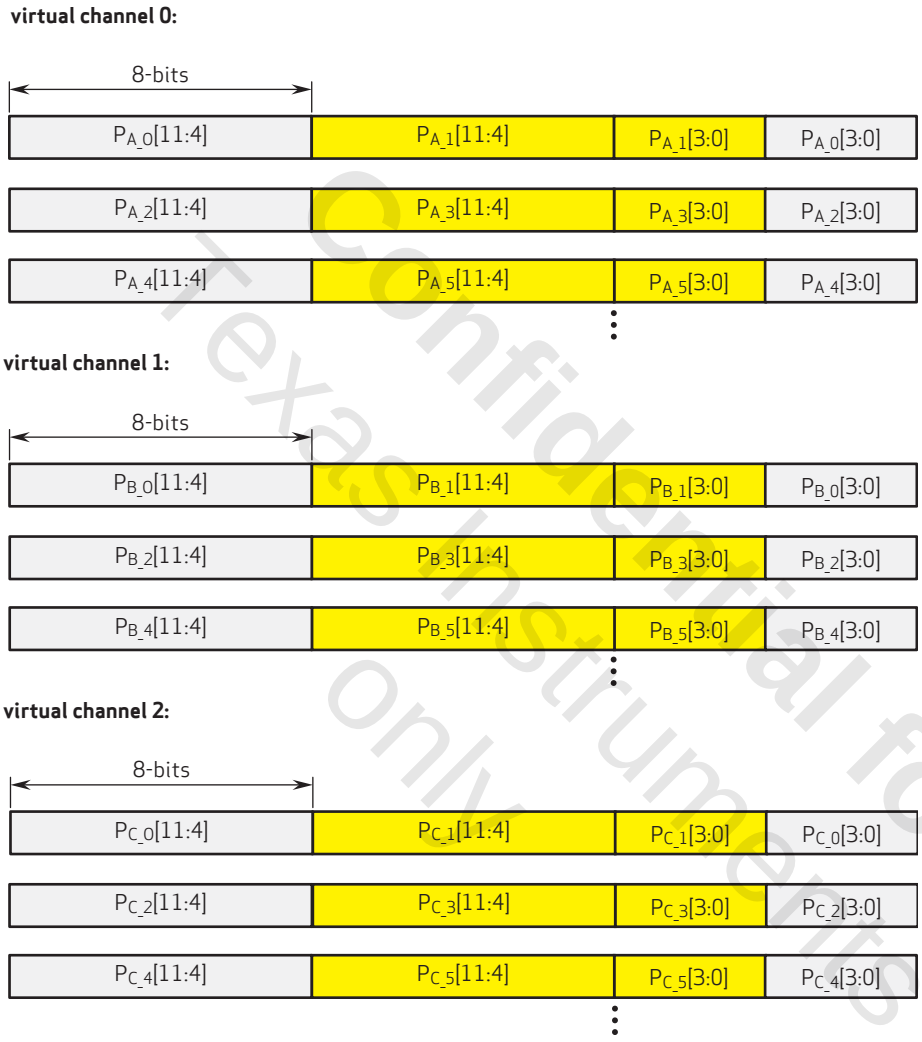


5.3.1.4 3x12b (3x10b) HDR

Three values per pixel: P_A (12-bit HCG), P_B (12-bit LCG), P_C (12-bit RAW VS)

In 10-bit mode, data is PWL compressed and MIPI 10b protocol is used.

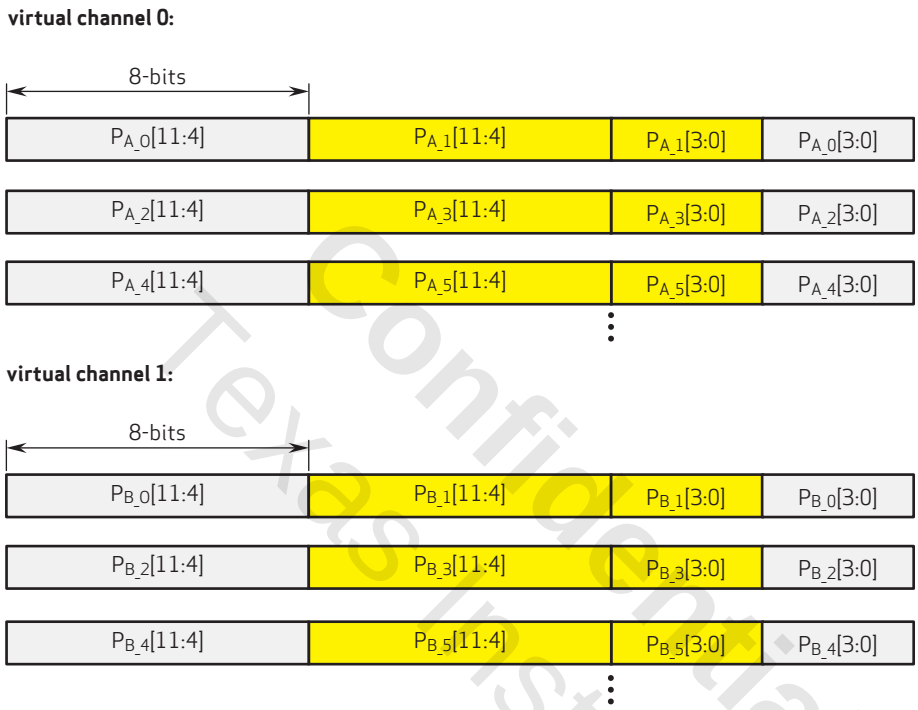
figure 5-14 3x12b (3x10b) HDR diagram



5.3.1.5 12b (10b) RAW DCG (HCG or LCG) + 12b (10b) VS dual HDR

Two values per pixel: P_A (12-bit HCG/LCG), P_B (12-bit RAW VS)

figure 5-15 12b RAW DCG (HCG or LCG) + 12b VS dual HDR diagram



5.3.1.6 16b DCG single HDR

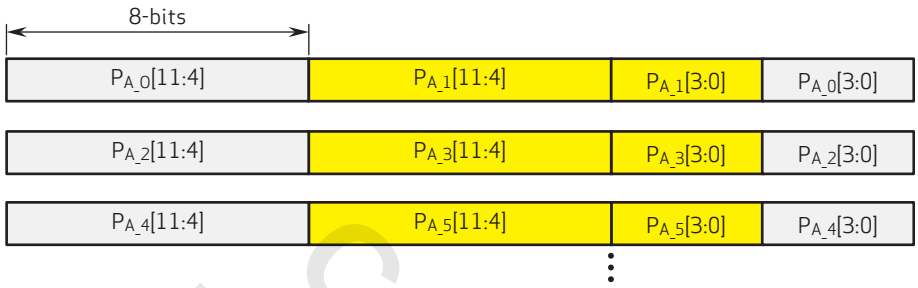
One value per pixel: P_A (16-bit combined DCG)

figure 5-16 16b DCG single HDR diagram

5.3.1.7 12b compressed DCG single HDR

One value per pixel: P_A (12-bit, compressed from 16-bit combined DCG)

figure 5-17 12b compressed DCG single HDR diagram



5.3.1.8 2x12b single HDR (VC0/VC1)

Two values per pixel: P_A (12-bit HCG), P_B (12-bit LCG)

figure 5-18 2x12b single HDR (VC0/VC1) diagram

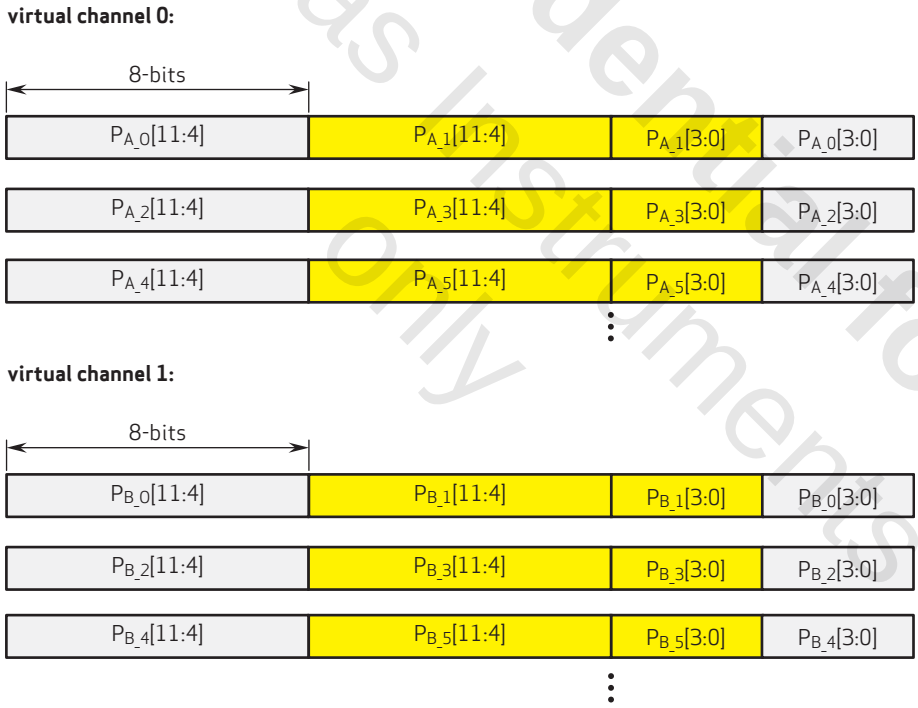


table 5-6 MIPI control registers (sheet 1 of 12)

address	register name	default value	R/W	description
0x31D0	CLK_POST_CONST_MIN	0x3C	RW	T(clk_post) Constant Minimum Value Default Value: 60 ns
0x31D1	CLK_POST_UI_MIN	0x34	RW	T(clk_post) UI Minimum Value Default Value: 52 UIs
0x31D2	CLK_TRAIL_CONST_MIN	0x3C	RW	T(clk_trail) Constant Minimum Value Default Value: 60 ns
0x31D3	CLK_TRAIL_UI_MIN	0x00	RW	T(clk_trail) UI Minimum Value Default Value: 0 UI
0x31D4	CLK_PREPARE_CONST_MIN	0x2D	RW	T(clk_prepare) Constant Minimum Value Default Value: 38 ns
0x31D5	CLK_PREPARE_UI_MIN	0x00	RW	T(clk_prepare) UI Minimum Value Default Value: 0 UIs
0x31D6	CLK_ZERO_CONST_MIN1	0x01	RW	T(clk_zero) Constant Minimum Value (High 2 Bits)
0x31D7	CLK_ZERO_CONST_MIN2	0x06	RW	T(clk_zero) Constant Minimum Value (Low 8 Bits) Default Value: 44 ns
0x31D8	CLK_ZERO_UI_MIN	0x00	RW	T(clk_zero) UI Minimum Value Default Value: 0 UIs
0x31D9	HS_EXIT_CONST_MIN	0x64	RW	T(hs_exit) Constant Minimum Value Default Value: 100 ns
0x31DA	HS_EXIT_UI_MIN	0x00	RW	T(hs_exit) UI Minimum Value Default Value: 0 UI
0x31DB	HS_PREPARE_CONST_MIN	0x28	RW	T(hs_prepare) Constant Minimum Value, Default Value: 40 ns
0x31DC	HS_PREPARE_UI_MIN	0x04	RW	T(hs_prepare) UI Minimum Value Default Value: 4 UI
0x31DD	HS_ZERO_CONST_MIN	0x69	RW	T(hs_zero) Constant Minimum Value, Default Value: 105 ns
0x31DE	HS_ZERO_UI_MIN	0x0A	RW	T(hs_zero) UI Minimum Value Default Value: 6 UI
0x31DF	HS_TRAIL_CONST_MIN	0x3C	RW	T(hs_trail) Constant Minimum Value Default Value: 65 ns
0x31E0	HS_TRAIL_UI_MIN	0x04	RW	T(hs_trail) UI Minimum Value Default Value: 4 UI
0x31E1	LPX_CONST_MIN	0x32	RW	T(lpx) Constant Minimum Value Default Value: 50 ns

table 5-6 MIPI control registers (sheet 2 of 12)

address	register name	default value	R/W	description
0x31E2	LPX_UI_MIN	0x00	RW	T(lpx) UI Minimum Value Default Value: 0 UI
0x31E3	MIPI_CLK_PERIOD1	0x00	RW	Clock Period of mipi_clk Used to calculate timing parameters of MIPI TX (low 2 bits, fraction). User may update this register when mipi_clk clock cycle is changed. mipi_clk default is 125.0 MHz
0x31E4	MIPI_CLK_PERIOD2	0x08	RW	Clock Period of mipi_clk Used to calculate timing parameters of MIPI TX (high 8 bits, integer). Default value: 8.00ns. User may update this register when mipi_clk clock cycle is changed. mipi_clk default is 125.0 MHz

table 5-6 MIPI control registers (sheet 3 of 12)

address	register name	default value	R/W	description
0x31E5	MIPI_LANE_CTRL0	0x82	RW	Data/Clock Lane Control Register Bit[7]: ext_timing Finish lane transfer long packet data exactly 0: Send any dummy data in data lane when image line byte number (add 2 CRC byte) can not be divided by lane number, which means that there will be one dummy byte in some data lanes. 1: Do not send any dummy data in data lane, which means that trail data will be behind image data in each data lane. Bit[6]: clk_data_chg Clock lane data changes from 2'b01 to 2'b10 Bit[5]: dis_clk_lane (active high) Disable clock lane Bit[4]: line_sync_en Insert LS/LE in MIPI TX stream if this bit is set Bit[3]: frame_cnt_zero_c1 MIPI TX channel 1 will keep frame counter zero if this bit is set Bit[2]: frame_cnt_zero_c0 MIPI TX channel 0 will keep frame counter zero if this bit is set Bit[1]: gate_clk_en2 (active high) Gate clock of clock lane when frame blanking time Bit[0]: gate_clk_en1 (active high) Gate clock of clock lane when line/frame blanking time mipi_lpkt_man 0x00 MIPI TX long packet manual mode. Default value: 8'h00
0x31E6	MIPI_LPKT_MAN	0x00	RW	MIPI TX Long Packet Manual Mode Bit[6]: lpkt_man_en Long packet manual input Bit[5:0]: dt_manual Manual data type
0x31E7	MIPI_DI0	0x30	RW	MIPI Data Identifier Register 0 (RAW16) Bit[7:6]: vc_num0 Virtual channel ID for data path 0 Bit[5:0]: img_dt0 Data type for data path 0

table 5-6 MIPI control registers (sheet 4 of 12)

address	register name	default value	R/W	description
0x31E8	MIPI_DI1	0x6C	RW	MIPI Data Identifier Register 1 (RAW12) Bit[7:6]: vc_num1 Virtual channel ID for data path 0 Bit[5:0]: img_dt1 Data type for data path 0
0x31E9	MIPI_DI2	0xAC	RW	MIPI Data Identifier Register 2 (RAW12) Bit[7:6]: vc_num2 Virtual channel ID for data path 0 Bit[5:0]: img_dt2 Data type for data path 0
0x31EA	MIPI_DI3	0xEC	RW	MIPI Data Identifier Register 3 (RAW12) Bit[7:6]: vc_num3 Virtual channel ID for data path 0 Bit[5:0]: img_dt3 Data type for data path 0
0x31EB	MIPI_EMB	0x3F	RW	MIPI Embedded Data Identifier Bit[6]: use_emb_data_type Use embedded data type for embedded data rows Bit[5:0]: emb_dt Data type for embedded data
0x31EC	MIPI_IMG_WIDTHH0	0x0B	RW	Bit[7:0]: img_width[15:8] Channel 0 image width high byte
0x31ED	MIPI_IMG_WIDTHL0	0x00	RW	Bit[7:0]: img_width[7:0] Channel 0 image width low byte
0x31EE	MIPI_IMG_HEIGHTH0	0x03	RW	Bit[7:0]: img_height[15:8] Channel 0 image height high byte
0x31EF	MIPI_IMG_HEIGHTL0	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 0 image height low byte
0x31F0	MIPI_IMG_WIDTHH1	0x05	RW	Bit[7:0]: img_width[15:8] Channel 1 image width high byte
0x31F1	MIPI_IMG_WIDTHL1	0x80	RW	Bit[7:0]: img_width[7:0] Channel 1 image width low byte
0x31F2	MIPI_IMG_HEIGHTH1	0x03	RW	Bit[7:0]: img_height[15:8] Channel 1 image height high byte
0x31F3	MIPI_IMG_HEIGHTL1	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 1 image height low byte
0x31F4	MIPI_IMG_WIDTHH2	0x05	RW	Bit[7:0]: img_width[15:8] Channel 2 image width high byte
0x31F5	MIPI_IMG_WIDTHL2	0x80	RW	Bit[7:0]: img_width[7:0] Channel 2 image width low byte

table 5-6 MIPI control registers (sheet 5 of 12)

address	register name	default value	R/W	description
0x31F6	MIPI_IMG_HEIGHTH2	0x03	RW	Bit[7:0]: img_height[15:8] Channel 2 image height high byte
0x31F7	MIPI_IMG_HEIGHTL2	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 2 image height low byte
0x31F8	MIPI_IMG_WIDTHH3	0x05	RW	Bit[7:0]: img_width[15:8] Channel 3 image width high byte
0x31F9	MIPI_IMG_WIDTHL3	0x80	RW	Bit[7:0]: img_width[7:0] Channel 3 image width low byte
0x31FA	MIPI_IMG_HEIGHTH3	0x03	RW	Bit[7:0]: img_height[15:8] Channel 3 image height high byte
0x31FB	MIPI_IMG_HEIGHTL3	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 3 image height low byte
0x31FC	MIPI_STATUS	–	R	MIPI Status Register Bit[1]: mipi_ph_done MIPI has transferred long packet header data. User can modify data type. Bit[0]: mipi_busy MIPI is transmitting data if this bit is assert

table 5-6 MIPI control registers (sheet 6 of 12)

address	register name	default value	R/W	description
0x31FD	MIPI_LANE_CTRL1	0xCB	RW	MIPI Data Lane Control Register 1 Bit[7]: hs_zero_sync_en 0: Send hs_en one cycle ahead of hs_zero state 1: Send hs_en sync with hs_zero state Bit[6]: sof_send_fs Send FS packet after MIPI received SOF 0: Send FS packet when VFIFO data is ready 1: Send FS packet when MIPI received SOF Bit[5]: chksum_exchg Long packet checksum byte exchange enable 0: Chksum = CRC[15:0] 1: Chksum = (CRC[7:0], CRC[15:8]) Bit[3]: lp_state Low power state when data lane is idle 0: Low power signal for each data lane may be controlled by lane_en. That means, if related lane_en is active, low power state of this data lane will stay 1 as idle. Other non-active lanes will stay 0 1: lp_p or lp_n will stay 1 if current data lane is not active Bit[2]: pclk_inv_en PCLK inverse enable, active high (output to PHY) Bit[1]: gen_fe_en1 Force to generate frame end short packet in channel 1 when MIPI TX has transmitted one line if VFIFO of this channel is overflow Bit[0]: gen_fe_en0 Force to generate frame end short packet in channel 0 when MIPI TX has transmitted one line if VFIFO of this channel is overflow

table 5-6 MIPI control registers (sheet 7 of 12)

address	register name	default value	R/W	description
0x31FE	MIPI_LANE_CTRL2	0x0F	RW	MIPI Data Lane Control Register 2 Bit[7]: d4_inv_en Data lane 4 inverse enable Bit[6]: d3_inv_en Data lane 3 inverse enable Bit[5]: d2_inv_en Data lane 2 inverse enable Bit[4]: d1_inv_en Data lane 1 inverse enable Bit[3]: lane4_en Data lane 4 enable Bit[2]: lane3_en Data lane 3 enable Bit[1]: lane2_en Data lane 2 enable Bit[0]: lane1_en Data lane 1 enable

table 5-6 MIPI control registers (sheet 8 of 12)

address	register name	default value	R/W	description
0x31FF	MIPI_LANE_CTRL3	0x03	RW	MIPI Data Lane Control Register 3 Bit[7]: ch3_crop_en Channel 3 crop enable 0: Channel 3 crop disable 1: Channel 3 crop enable Bit[6]: ch2_crop_en Channel 2 crop enable 0: Channel 2 crop disable 1: Channel 2 crop enable Bit[5]: ch1_crop_en Channel 1 crop enable 0: Channel 1 crop disable 1: Channel 1 crop enable Bit[4]: ch0_crop_en Channel 0 crop enable 0: Channel 0 crop disable 1: Channel 0 crop enable Bit[3]: fcnt_zero_c3 MIPI TX channel 3 will keep frame counter zero if this bit is set Bit[2]: fcnt_zero_c2 MIPI TX channel 2 will keep frame counter zero if this bit is set Bit[1]: gen_fe_en3 Force to generate frame end short packet in channel 3 when MIPI TX has transmitted one line if VFIFO of this channel is overflow Bit[0]: gen_fe_en2 Force to generate frame end short packet in channel 2 when MIPI TX has transmitted one line if VFIFO of this channel is overflow

table 5-6 MIPI control registers (sheet 9 of 12)

address	register name	default value	R/W	description
0x3200	MIPI_TEST_MODE	0x00	RW	MIPI TX Test Mode Bit[5]: lp_n_man_data Output manual lower power data in MIPI TX test mode Bit[4]: lp_p_man_data Output manual lower power data in MIPI TX test mode Bit[3]: lp_man_en Output manual low power data enable in low power test mode and de-assert high speed signal (hs_en or valid) Bit[2]: hs_man_en Manual test data will output to PHY when this bit is set and MIPI TX in high speed test mode Bit[1]: test_mode 0: Test start point sync by mipi_test 1: Test start point sync by MIPI RX prbs_en Bit[0]: mipi_test (active high) Test MIPI TX and RX PHY
0x3201	MANUAL_TEST_DATA	0xFF	RW	Manual Test Data for MIPI PHY
0x3202	MIPI_TEST_CFG	0x00	RW	MIPI Test Configuration Bit[1:0]: rx_prbs_en Enable MIPI PHY test including RX PHY and TX PHY
0x3203	MAX_FRAME_CNTH0	0xFF	RW	Maximum Frame Counter of Channel 0 High Byte
0x3204	MAX_FRAME_CNTL0	0xFF	RW	Maximum Frame Counter of Channel 0 Low Byte
0x3205	MAX_FRAME_CNTH1	0xFF	RW	Maximum Frame Counter of Channel 1 High Byte
0x3206	MAX_FRAME_CNTL1	0xFF	RW	Maximum Frame Counter of Channel 1 Low Byte
0x3207	MAX_FRAME_CNTH2	0xFF	RW	Maximum Frame Counter of Channel 2 High Byte
0x3208	MAX_FRAME_CNTL2	0xFF	RW	Maximum Frame Counter of Channel 2 Low Byte
0x3209	MAX_FRAME_CNTH3	0xFF	RW	Maximum Frame Counter of Channel 3 High Byte

table 5-6 MIPI control registers (sheet 10 of 12)

address	register name	default value	R/W	description
0x320A	MAX_FRAME_CNTL3	0xFF	RW	Maximum Frame Counter of Channel 3 Low Byte
0x320B	YUV422_12B_DT	0x1B	RW	YUV422_12b Data Type
0x320C	YUV422_10B_DT	0x1F	RW	YUV422_10b Data Type
0x320D	YUV422_8B_DT	0x1E	RW	YUV422_8b Data Type
0x320E	RAW16_DT	0x30	RW	RAW16 Data Type
0x320F	RAW14_DT	0x2D	RW	RAW14 Data Type
0x3210	RAW12_DT	0x2C	RW	RAW12 Data Type
0x3211	RAW10_DT	0x2B	RW	RAW10 Data Type
0x3212	RAW8_DT	0x2A	RW	RAW8 Data Type
0x3213	RGB888_DT	0x24	RW	RGB888 Data Type
0x3214	RGB565_DT	0x22	RW	RGB565 Data Type

table 5-6 MIPI control registers (sheet 11 of 12)

address	register name	default value	R/W	description
0x3215	DAT_SEQ_CTRL	0x00	RW	Data Sequence Control Bit[7:5]: total_seq RGB sequence 000: BGR 001: BRG 010: GBR 011: GRB 100: RGB 101: RBG Bit[4:3]: high_half_seq Quarter sequence Used to adjust each 12-bits data sequence 00: Data[11:0] 01: (Data[9:0], data[11:10]) 10: (Data[7:0], data[11:8]) 11: Data[11:0] Bit[2]: low_half_seq Low half sequence Used to adjust low 24-bits data sequence 0: Data[23:0] 1: (Data[11:0], data[23:12]) Bit[1]: quarter_seq High half sequence Used to adjust low 24-bits data sequence 0: Data[47:24] 1: (Data[35:24], data[47:36]) Bit[0]: rgb_seq Total sequence 0: Data[47:0] 1: (Data[11:0], data[23:12], data[35:24], data[47:36])
0x3216	LP_DELAY	0x04	RW	LP00~LP11 Delay Cycle When hs_zero Sync Enable
0x3217	MIPI_DATA_TAG0	0x30	RW	Data_ID Tag Transmitted in Virtual Channel 0 for Supporting "Same Image Data Transmit in Different Virtual Channel with Different Data_ID Tag" Case
0x3218	MIPI_DATA_TAG1	0x6C	RW	Data_ID Tag Transmitted In Virtual Channel 1 for Supporting "Same Image Data Transmit in Different Virtual Channel with Different Data_ID Tag" Case

table 5-6 MIPI control registers (sheet 12 of 12)

address	register name	default value	R/W	description
0x3219	MIPI_DATA_TAG2	0xAC	RW	Data_ID Tag Transmitted in Virtual Channel 2 for Supporting "Same Image Data Transmit in Different Virtual Channel with Different Data_ID Tag" Case
0x321A	MIPI_DATA_TAG3	0xEC	RW	Data_ID Tag Transmitted in Virtual Channel 3 for Supporting "Same Image Data Transmit in Different Virtual Channel with Different Data_ID Tag" Case
0x321B	USE_VFIFO_TYPE	0x00	RW	Use Size Signals (12, 10, and 8) from VFIFO

5.3.2 DVP

The OV9716 can output pixel data on a 12-bit DVP bus. The exposures are staggered in multiple exposure output mode. When one of the exposures are in vertical blanking, the time slot for this pixel data will be padded and thus invalid. In DVP mode, VSYNC indicates start of HCG/LCG-exposure output and HREF indicates that pixel data is output on DVP (either HCG/LCG, VS, or both).

HREF, VSYNC, and PCLK are configured as video output port by default as shown in **figure 5-20**. The leading edge of VSYNC is triggered by an internal SOF signal and the interval between the internal SOF signal and VSYNC is controlled by v_sync_delay (0x31B4~0x31B6 in unit of PCLK periods). VSYNC pulse width is set by registers 0x31B0~0x31B3 as in the following formula:

VSYNC width = [VSYNC width line × t_{Row}] + [VSYNC width pixel × t_{PCLK}]

where:

t_{Row} is row period

t_{PCLK} is PCLK period

VSYNC width line - {0x31B0, 0x31B1}

VSYNC width pixel - {0x31B2, 0x31B3}

figure 5-19 DVP setup/hold time diagram

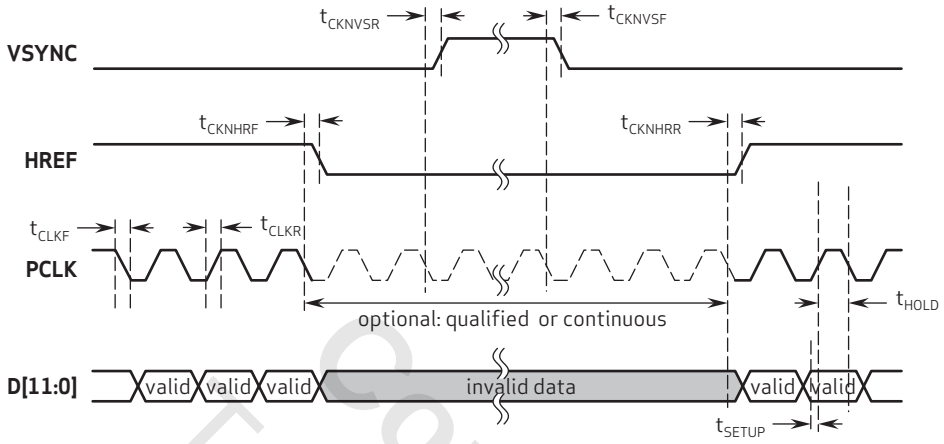
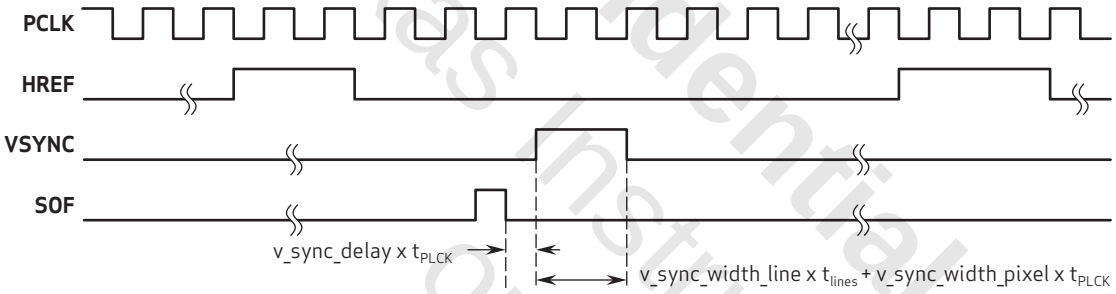


figure 5-20 DVP diagram



The OV9716 supports walking one test pattern to test the connection between the sensor and the backend processor. The test pattern is enabled by register 0x31B8[0]. By default, the image data bits are aligned with pins D[11:0].

The driver strength of the DVP can be configured by 0x3488[1:0].

The DVP output is qualified by VSYNC and HREF and the timing is shown in **figure 5-21**.

table 5-7 DVP setup/hold time[ab] (sheet 1 of 2)

symbol	parameter	min	typ	max	unit
t_{CKNVSR}	PCLK falling edge to VSYNC rising edge delay	–	1.91	–	ns
t_{CKNVSF}	PCLK falling edge to VSYNC falling edge delay	–	0.97	–	ns
t_{CKNHRF}	PCLK falling edge to HREF falling edge delay	–	0.18	–	ns
t_{CKNHRR}	PCLK falling edge to HREF rising edge delay	–	-0.11	–	ns

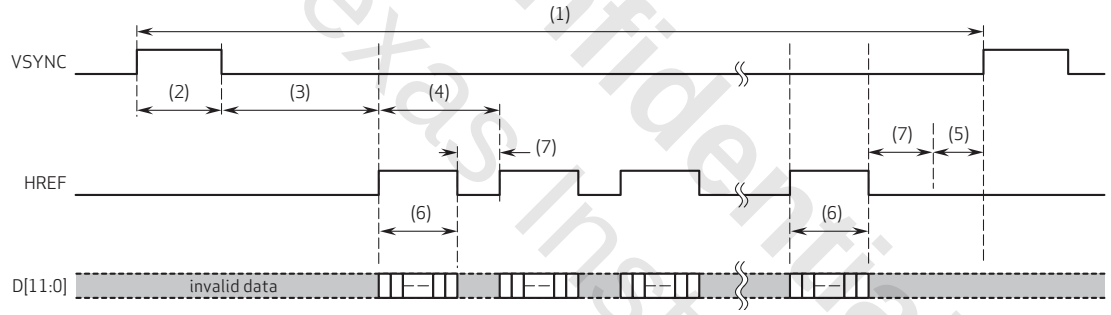
table 5-7 DVP setup/hold time[ab] (sheet 2 of 2)

symbol	parameter	min	typ	max	unit
t_{CLKF}	PCLK fall time	–	1.22	–	ns
t_{CLKR}	PLCK rise time	–	2.41	–	ns
t_{SETUP}	data setup time	4.22	4.50	4.81	ns
t_{HOLD}	data hold time	4.99	5.26	5.50	ns

a. measured at 1.8V DOVDD and 96 MHz PCLK, with 2x drive strength

b. timing measurement shown at beginning of rising edge and/or end of falling edge signifies 10%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge and/or beginning of falling edge signifies 90%

figure 5-21 DVP timing diagram



(1) frame period

(2) VSYNC width

(3) VSYNC to HREF

(4) line period

(5) HREF to VSYNC

(6) active pixel

(7) horizontal blanking

(8) last horizontal blanking to VSYNC high

VSYNC pulse width is programmable from 1 CLK to 1 frame (high period = #lines + #pixels): registers 0x31B0~0x31B1: #lines, registers 0x31B2~0x31B3: #pixels

N = VS-delay in whole rows × image width

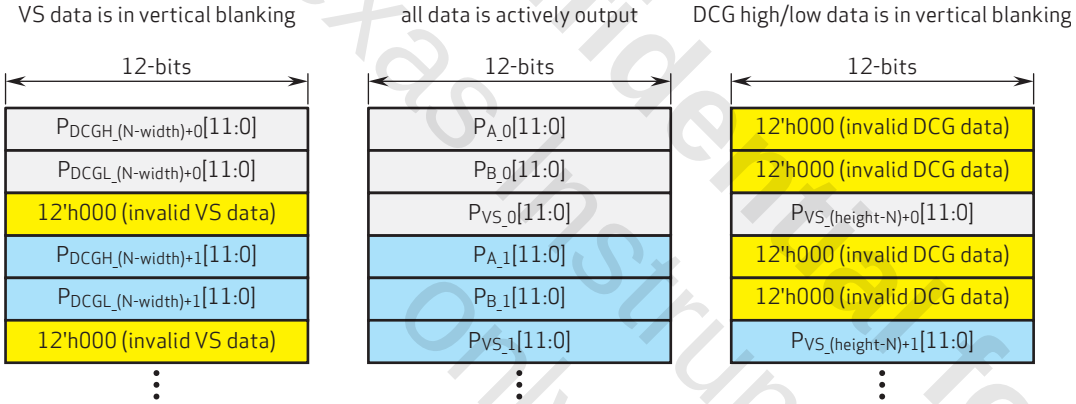
Height = rows × image width

table 5-8 supported output formats and frame rates for DVP

maximum frame rate supported via DVP (100 MHz) interface			
format		resolution	max frame rate
linear	12b	1392 x 976	30 fps
dual exposure HDR	12b compressed DCG+12b VS	1280 x 720	30 fps
	12b RAW (HCG or LCG)+ 12b VS		30 fps
single exposure HDR	12b compressed DCG	1392 x 976	30 fps
	2x12b	1280 x 960	30 fps

table 5-8 represents the resolution and maximum frame rate for DVP with different output format.

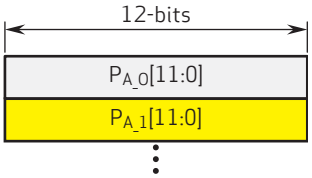
figure 5-22 staggered HDR with DVP diagram



5.3.2.1 12 bits linear mode

One value per pixel: P_A (12-bit RAW)

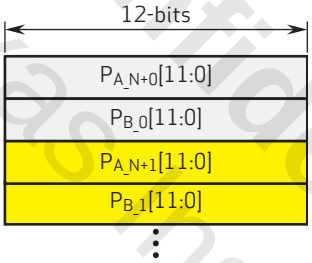
figure 5-23 12 bits linear mode diagram



5.3.2.2 12b RAW (HCG or LCG) + 12b VS dual HDR

Two values per pixel: P_A (12-bit HCG or LCG), P_B (12-bit RAW VS)

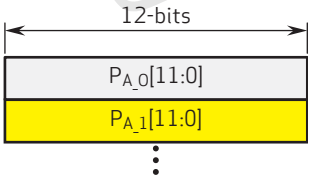
figure 5-24 12b RAW (HCG or LCG) + 12b VS diagram



5.3.2.3 12b compressed DCG single HDR

One value per pixel: P_A (12-bit, compressed from 16-bit)

figure 5-25 single exposure HDR diagram



5.3.2.4 2x12b single HDR

Two values per pixel: P_A (12-bit HCG), P_B (12-bit LCG)

figure 5-26 2x12b single HDR diagram

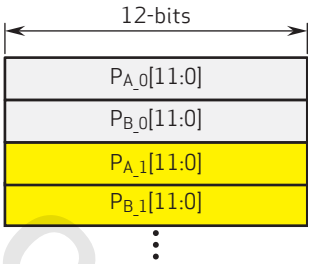


table 5-9 DVP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x31B0	VSYNC_WIDTH_LINE_H	0x00	RW	VSYNC Width by Line Number High Byte
0x31B1	VSYNC_WIDTH_LINE_L	0x00	RW	VSYNC Width by Line Number Low Byte
0x31B2	VSYNC_WIDTH_PIXEL_H	0x02	RW	VSYNC Width by Pixel Number High Byte
0x31B3	VSYNC_WIDTH_PIXEL_L	0x00	RW	VSYNC Width by Pixel Number Low Byte
0x31B4	VSYNC_DELAY_H	0x00	RW	VSYNC Delay Count High Byte
0x31B5	VSYNC_DELAY_M	0x01	RW	VSYNC Delay Count Middle Byte
0x31B6	VSYNC_DELAY_L	0x00	RW	VSYNC Delay Count Low Byte
0x31B7	POLARITY_CTRL	0x00	RW	Polarity Control Register Bit[6]: bit_reverse_enable Invert output bits Bit[2]: href_polarity 0: Active high 1: Active low Bit[1]: vsync_polarity 0: Active high 1: Active low Bit[0]: pclk_polarity Output inverted PCLK

table 5-9 DVP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x31B8	TEST_ORDER	0x00	RW	Test Pattern Mode Bit[3]: test_mode When set, only change data every other clock Bit[2]: test_bit10 Enable 10-bit test Bit[1]: test_bit8 Enable 8-bit test Bit[0]: test_enable Enable test
0x31B9	BYP_SELECT	0x00	RW	Bypass Select Bit[5]: data_bit_shift Used in test mode to select between bit swap methods when using 16 bits Bit[4:0]: Not used
0x31BA	R_FIFO	0x00	RW	Top Sync FIFO Control Bit[1]: dvp_sync_pclk_pol Invert output PCLK within DVP_SYNC module Bit[0]: dvp_sync_pll_pclk_inv Invert input PLL PCLK within DVP_SYNC module

5.4 instructions for backend control

5.4.1 VS data path delay

In staggered mode, VS VSYNC/FS has specific numbers of rows delay after HCG/LCG VSYNC/FS as shown in **figure 5-27**.

vs_dp_delay=integer(TexpVS)+vs_sample_delay

where vs_dp_delay is the time delay between HCG/LCG VSYNC/FS and VS VSYNC/FS, which is defined by integer part of VS exposure time TexpVS plus vs_sample_delay (value between 0 and 2). Value is in units of row time. vs_dp_delay value can be read from register as shown in **table 5-10**.

figure 5-27 sensor frame control signals diagram

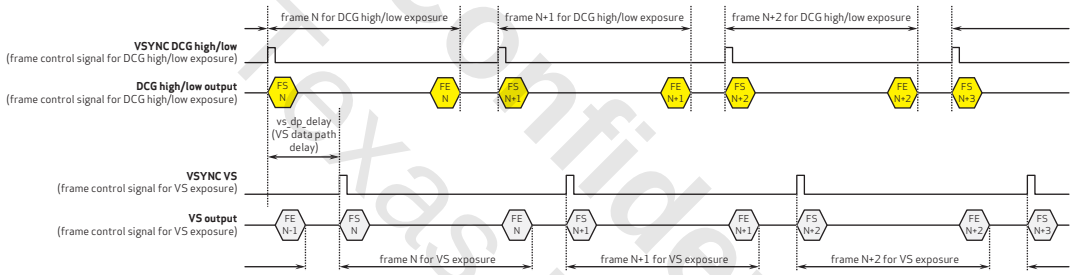


table 5-10 VS data path delay registers

address	register name	default value	R/W	description
0x30CE	VS_DP_DELAY_H	–	R	Current Frame Very Short Data Path Delay in Rows High Byte
0x30CF	VS_DP_DELAY_L	–	R	Current Frame Very Short Data Path Delay in Rows Low Byte

In DVP mode, there is no FS and FE packet data. The user has to find the VS data by reading vs_dp_delay register in embedded data that specify this number of rows delay for VS output and then count the number of HREF until VS data is valid. Similar to MIPI without virtual channel mode, the user must read vs_dp_delay to define the quantities of dummy row data.

5.5 register writing

5.5.1 suggestion for writing register value just after VSYNC or FS

In order to avoid register setting for one frame being split into two frames by mistake, the register value should be written as early as possible after VSYNC or FS. If register values are written during frame N, new parameters can be seen in frame:

- N+1: WB gain and LENC
- N+2: exposure, analog gain, digital gain, and conversion gain

5.6 embedded data

Additional information about the set up and configuration of the sensor can be embedded in the video stream. The embedded data contains the values of a programmable list of registers to describe the current state of the sensor (e.g., frame counter, exposure time and gain, etc.). The embedded data is added before the video stream. Embedded data can be enabled in the image by setting register 0x30C1[2], and the output size must be increased by 2 to output 2 embedded rows.

In linear mode, only one row embedded data is supported. Row two will be blank data.

5.6.1 embedded data format at output

Each register value is preceded by the tag 0xDA. When output data width is more than 8 bits, tag and register values will be MSB aligned.

When more than one capture is transmitted, embedded data is only added to the first capture. Blank data is added in the embedded row for the rest of the captures. For example, embedded data will be added in the HCG captures for 3x12b and in the LCG captures for 12b LCG +12b VS.

The number of registers transmitted is dependent on the register start and end address and might be one or two rows. The last four registers are CRC value (4 bytes) preceded with the tag value before each byte. The range of registers, selected as embedded data, will be output in incrementing order from start to end address. The embedded data row will automatically continue on the next row. When the whole range has been output, the CRC data will be appended. If the requested range does not fit within two embedded data rows, the range will be truncated with an appended CRC value. If CRC3 is not the end of the embedded rows, it will be terminated with 'h00.

5.6.1.1 bit alignment

10 bits data (compressed from 12 bits data):

{Embedded data, 2'h0}

12 bits data (DCG compressed or linear mode):

{Embedded data, 4'h0}

16 bits (data packed as 2 x 8 bits words)

{Embedded data, 8'h00}

figure 5-28 embedded data layout diagram

table 5-11 embedded data registers

address	register name	default value	R/W	description
0x3468	EMB_START_ADDR0_H	0x30	RW	First Embedded Data Range High Byte
0x3469	EMB_START_ADDR0_L	0x00	RW	First Embedded Data Range Low Byte
0x346A	EMB_END_ADDR0_H	0x35	RW	Last Embedded Data Range High Byte
0x346B	EMB_END_ADDR0_L	0x00	RW	Last Embedded Data Range Low Byte

5.7 group hold

The OV9716 supports a group hold function where the register values are recorded in an internal buffer instead of writing to the register directly. The group hold function is controlled through registers 0x3460~0x346D.

The OV9716 supports up to four groups. The number of entries for each group is set by registers 0x3460~0x3463. The total sum for the four groups is limited to 256 registers. In manual mode, a register write burst can be triggered with a SCCB write and the specified group's register settings will be written to the register interface. In automatic mode, two groups are selected and the number of frames each group should be active. The sensor will continuously update the register settings accordingly.

To program group hold, set 0x3467 to 0x00 and select which group to program in 0x3464[3:2]. Then, specify the register to group hold by entering the register address and swap MSB (bit[15]) in address to 1. So, 0x3000 would be 0xB000, 0x30E6 would be 0xB0E6, etc.

To enable group hold, set register 0x3467[1:0] for 'single launch' to launch group settings once, or 'auto launch' to automatically switch between groups selected in 0x3464[3:0].

Group hold examples:

Set group0:

```
6C 3467 00;
6C 3464 00; select group 0 for record
6C B0B6 01; record registers for group launch by setting bit[15] of address to 1
```

Set group1:

```
6C 3467 00;
6C 3464 04; select group 1 for record
6C B0B6 02;
```

Set group2:

```
6C 3467 00;
6C 3464 08; select group 2 for record
6C B0B6 03;
```

Set group3:

```
6C 3467 00;
6C 3464 0C; select group 3 for record
6C B0B6 04;
```

Single launch group0:

```
6C 3464 10;
6C 3467 01; single launch
```

Single launch group1:

```
6C 3464 14;
6C 3467 01
```

Single launch group2:

```
6C 3464 18;
6C 3467 01;
```

Single launch group3:

```
6C 3464 1C;
6C 3467 01;
```

Auto switch between group0 and group1:

```
6C 3464 11; group0 and 1
6C 3467 02; auto launch
```

Auto switch between group0 and group2:

```
6C 3464 12; group 0 and 2
6C 3467 02; auto launch
```

Auto switch between group2 and group3:

```
6C 3464 1B; group 2 and 3
6C 3467 02; auto launch
```

table 5-12 group hold control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3460	GROUP_LENGTH0	0x40	RW	Number of Registers for Group 0, Total Sum of Four Groups is Limited to 256
0x3461	GROUP_LENGTH1	0x40	RW	Number of Registers for Group 1
0x3462	GROUP_LENGTH2	0x40	RW	Number of Registers for Group 2
0x3463	GROUP_LENGTH3	0x40	RW	Number of Registers for Group 3

table 5-12 group hold control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3464	GROUP_CTRL	0x03	RW	Group Control Register, Hold Control is Bit 15 of Address Bit[6]: launch_now Launch immediately, when single_start is set Bit[5]: launch_pre_sof Launch before sensor core SOF, if single_start is set Bit[4]: launch_post_sof Launch after sensor core SOF, if single_start is set Bit[3:2]: first_grp_sel Main group select for hold and launch operation. Also used as first group in auto mode 00: Group select 0 01: Group select 1 10: Group select 2 11: Group select 3 Bit[1:0]: second_grp_sel Used as second group in auto mode
0x3465	FIRST_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by First Group Select
0x3466	SECOND_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by Second Group Select
0x3467	OPERATION_CTRL	0x02	RW	Bit[1]: auto_mode Switches automatically between first and second groups using frame counts Bit[0]: single_start Launch only once, reset by logic after done, overriden by auto_mode
0x3468	EMB_START_ADDR0_H	0x30	RW	First Embedded Data Range High Byte
0x3469	EMB_START_ADDR0_L	0x00	RW	First Embedded Data Range Low Byte
0x346A	EMB_END_ADDR0_H	0x35	RW	Last Embedded Data Range High Byte
0x346B	EMB_END_ADDR0_L	0x00	RW	Last Embedded Data Range Low Byte
0x346C	ACTIVE_GROUP_NR	–	R	Indicates Which Group is Active
0x346D	FRAME_CNT_ACTIVE	–	R	Number of Frames with Current Group, Only Valid in Auto Mode

5.8 cyclic redundancy check

The OV9716 supports cyclic redundancy check (CRC-32C) on the embedded data and SCCB (CRC-16-IBM) communication.

5.8.1 embedded data

The CRC on embedded data is calculated using CRC-32C. The polynomials are 0x1EDC6F41 (normal). The last four registers are CRC value (4 bytes) preceded with tag value before each byte. The tag (0xDA) is not included in the CRC.

5.8.2 SCCB communication

The CRC on SCCB write is calculated using CRC-16-IBM. The polynomial is 0x8005. CRC is calculated on both the (register) address and data (in the order of 1: high address byte, 2: low address byte 3: data). An SCCB read operation to any of the CRC registers {0x7FF6, 0x7FF7} will reset the CRC calculation. The CRC registers will be reset on the next SCCB write operation (i.e., they hold the previous CRC value until a new SCCB write occurs after any of the CRC registers are read). CRC registers appear as part of embedded data (without being reset automatically).

table 5-13 SCCB CRC registers

address	register name	default value	R/W	description
0x7FF6	SCCB_CRC_H	–	R	SCCB CRC High Byte
0x7FF7	SCCB_CRC_L	–	R	SCCB CRC Low Byte

6 SCCB interface

The SCCB interface controls the image sensor operation.

6.1 SCCB timing

figure 6-1 SCCB interface timing

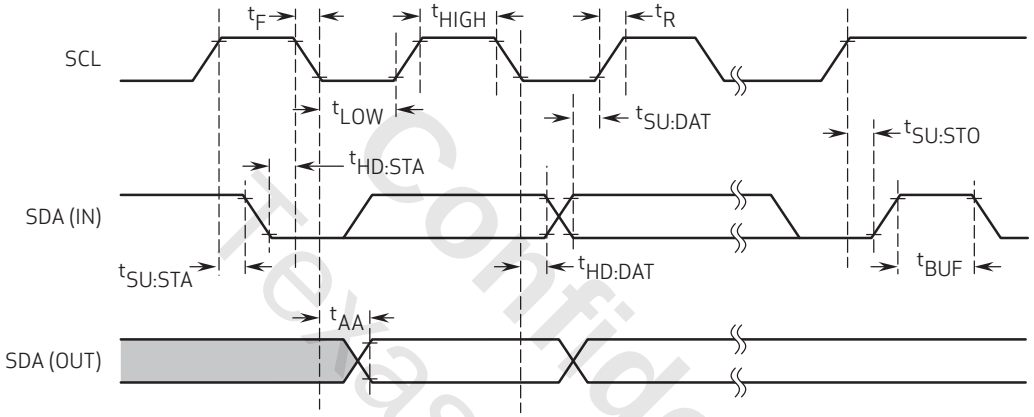


table 6-1 SCCB interface timing specifications[a]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency		400		kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs

a. timing measurement shown at beginning of rising edge or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge or beginning of falling edge signifies 70%

table 6-2 SCCB interface timing specifications based on 1000 kHz[a]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency		1000[b]		kHz
t_{LOW}	clock low period	0.5			µs
t_{HIGH}	clock high period	0.26			µs
t_{AA}	SCL low to data out valid			0.45	µs
t_{BUF}	bus free time before new start	0.5			µs
$t_{HD:STA}$	start condition hold time	0.26			µs
$t_{SU:STA}$	start condition setup time	0.26			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.5			µs
$t_{SU:STO}$	stop condition setup time	0.26			µs
t_R, t_F	SCCB rise/fall times			0.12	µs

a. timing measurement shown at beginning of rising edge or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge or beginning of falling edge signifies 70%

b. for 1000 kHz mode, minimum input clock is 10 MHz; for 400 kHz or less mode, minimum input clock is 6 MHz

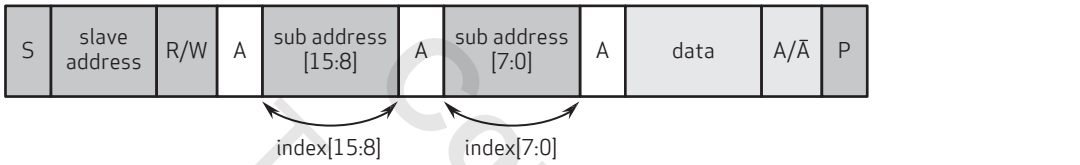
6.2 direct access mode

6.2.1 message format

The OV9716 supports the message format shown in **figure 6-2**. The repeated START (Sr) condition is shown in **figure 6-3** and **figure 6-5**.

figure 6-2 message type

message type: 16-bit sub-address, 8-bit data, and 8-bit slave address



from slave to master
from master to slave
direction depends on operation

S START condition
P STOP condition
Sr repeated START condition

A acknowledge
Ā negative acknowledge

6.2.2 read / write operation

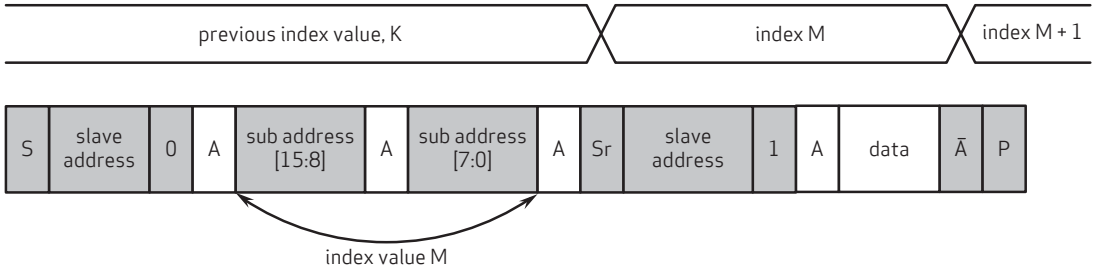
The OV9716 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

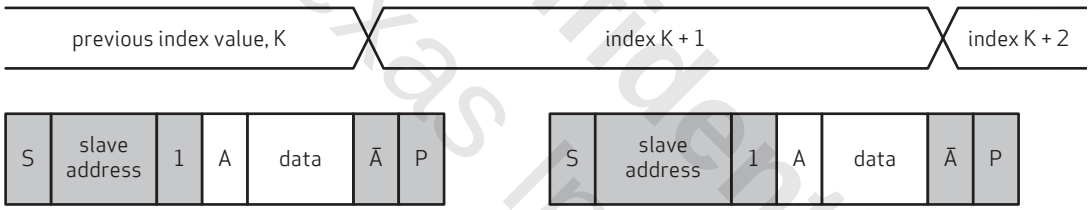
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 6-3**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-3 SCCB single read from random location



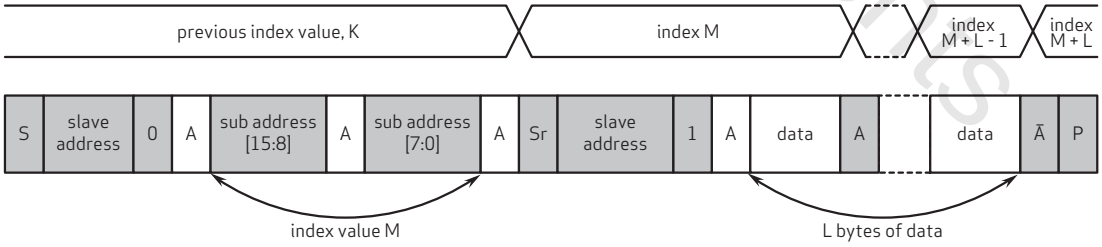
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 6-4**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-4 SCCB single read from current location



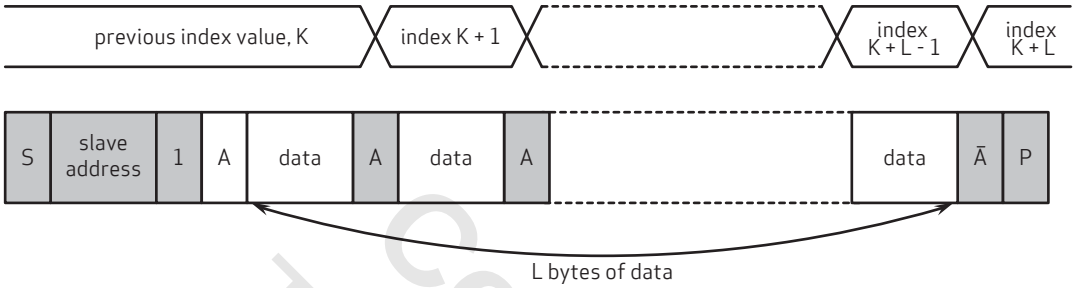
The sequential read from a random location is illustrated in **figure 6-5**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 6-5 SCCB sequential read from random location



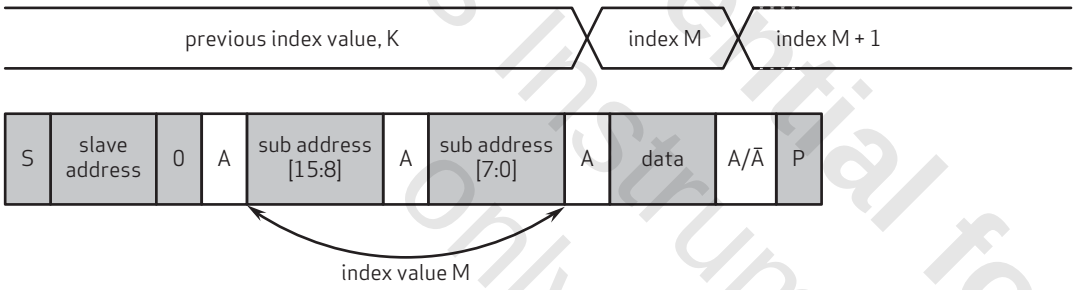
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation as shown in **figure 6-6**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 6-6 SCCB sequential read from current location



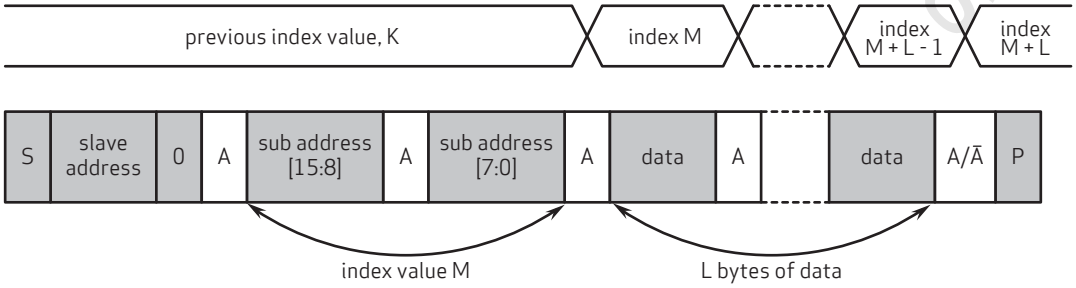
The write operation to a random location is illustrated in **figure 6-7**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 6-7 SCCB single write to random location



The sequential write is illustrated in **figure 6-8**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 6-8 SCCB sequential write to random location



7 one-time programmable (OTP) memory

The OV9716 has a total of 512 bytes of OTP memory. Using the auto load function, the data in the OTP memory is written to registers when sensor is powered up (e.g., temperature calibration data).

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-50°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-40°C to +132°C sensor junction temperature

a. sensor functions in the operating range; however, some image quality changes may be noticed at the temperature extremes

8.3 DC characteristics

table 8-3 DC characteristics (-40°C < T_J < 132°C)

symbol	parameter	min	typ	max @ 132°C	unit
supply					
$V_{DD-3.3}$	supply voltage (analog)	3.14	3.3	3.47	V
$V_{DD-1.2}$	supply voltage (digital circuit)	1.1	1.2	1.3	V
$V_{DD-1.8}$	supply voltage (digital I/O + AVDD)	1.7	1.8	1.9	V
$I_{DD-3.3}$	active (operating) current[a]		25	35	mA
$I_{DD-1.2}$			92	150	mA
$I_{DD-1.8}$			11	24	mA
$I_{DDS-PWDNB-3.3}$[b]	standby current[c]		60	70	µA
$I_{DDS-PWDNB-1.2}$			10	58	mA
$I_{DDS-PWDNB-1.8}$			40	70	µA
digital inputs (typical conditions: AVDD18 =1.8V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[d]	SCL and SDA	-0.5	0	0.54	V
V_{IH}[d]	SCL and SDA	1.26	1.8	2.3	V

a. active current based on 30 fps settings

b. standby current without input clock

c. standby current based on high temperature

d. based on DOVDD = 1.8V.

8.4 AC characteristics

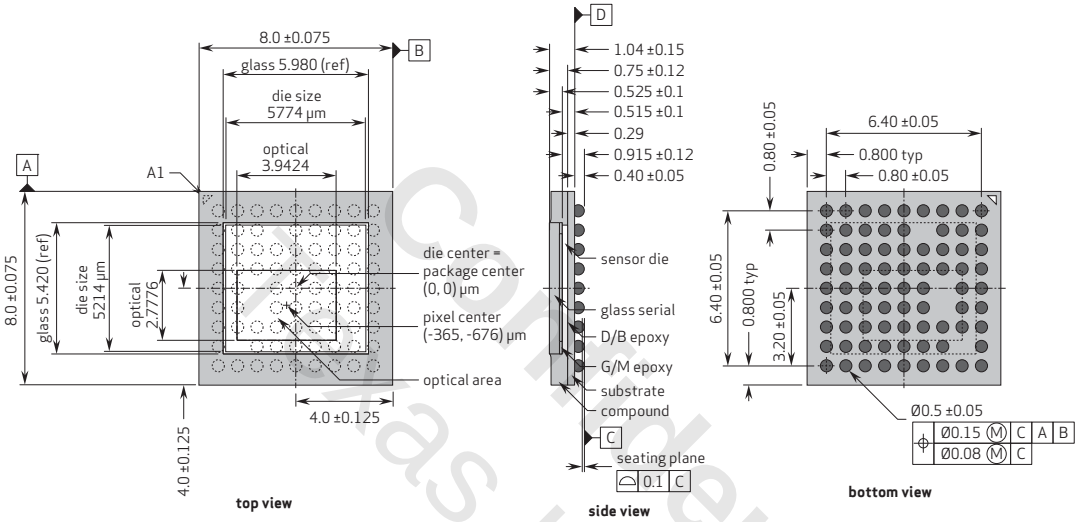
table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	36	MHz
t_r, t_f	clock input rise/fall time			5	ns

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications



note 1 all exposed metallized area shall be gold plated 0.5 µm min. thk. over nickel plated 5 µm min. thk.

note 2 seal area and die attach area shall be isolated from any leads

note 3 the bottom side is used solder mask define

note 4 substrate thickness: 0.29 mm

note 5 lid material: AR_AR coating glass 0.40 mm

note 6 wafer thickness = 0.200 mm (8 mils)

note 7 solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu)

note 8 dimensions apply to solder balls post reflow (solder ball diameter: 0.5 mm)

note 9 pixel center = package center

note 10 maximum rotation of optical area relative to package edges: 1°
maximum tilt of optical area relative to D: 25 microns
maximum tilt of optical area relative to top of cover glass: 50 microns

note 11 all dimension in millimeters unless otherwise specified

table 9-1 package dimensions (sheet 1 of 2)

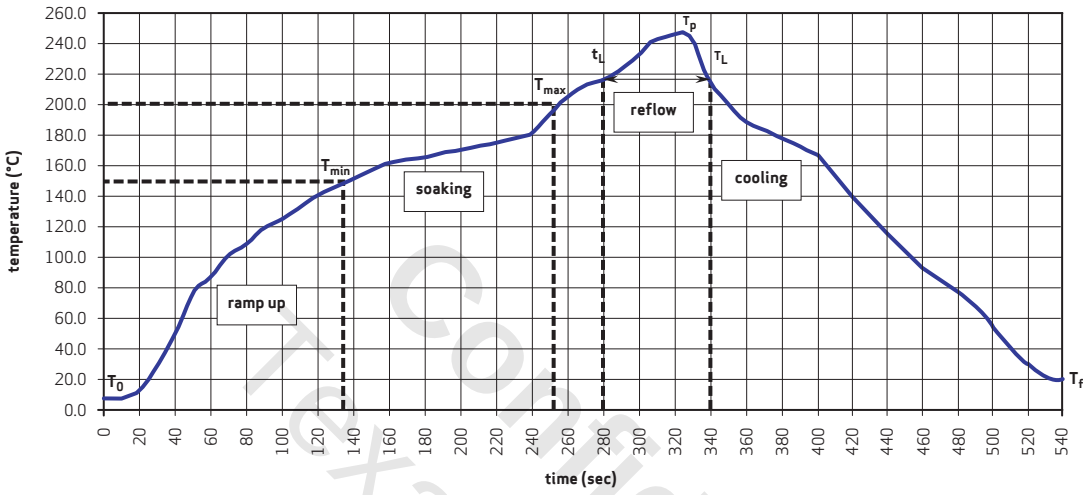
parameter	min	typ	max	unit
package body dimension x	7.925	8	8.075	mm
package body dimension y	7.925	8	8.075	mm
package height	1.24	1.44	1.64	mm

table 9-1 package dimensions (sheet 2 of 2)

parameter	min	typ	max	unit
ball height	0.35	0.4	0.45	mm
package body thickness	0.89	1.04	1.19	mm
thickness of glass surface to wafer	0.425	0.525	0.625	mm
image plane height	0.795	0.915	1.035	mm
ball diameter	0.45	0.5	0.55	mm
solder ball opening size		0.4		mm
total pin count		77 (12 NC)		
pin count x-axis		9		
pin count y-axis		9		
pins pitch x-axis	0.75	0.8	0.85	mm
pins pitch y-axis	0.75	0.8	0.85	mm
edge-to-pin center distance along x		0.8		mm
edge-to-pin center distance along y		0.8		mm
substrate thickness	0.24	0.29	0.34	mm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note The OV9716 uses a lead free package.

table 9-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5°C (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_P to T_L)	cooling from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling from 217°C to room temperature	temperature slope ≤ 6°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

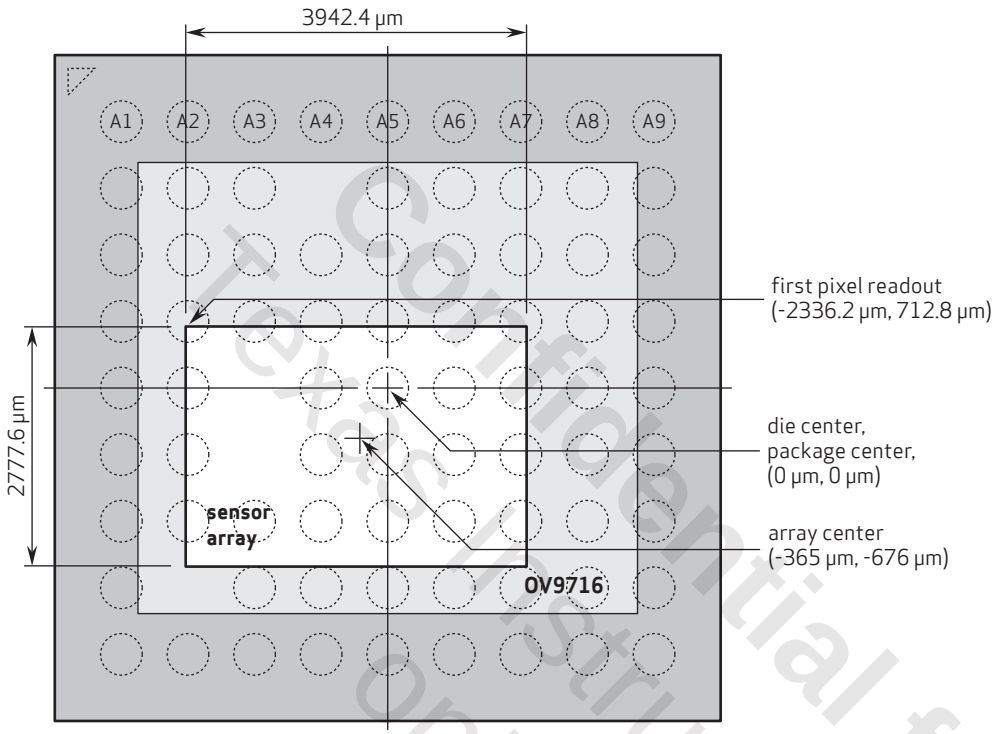
a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM<500 as recommendation

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A9 oriented down on the PCB.

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

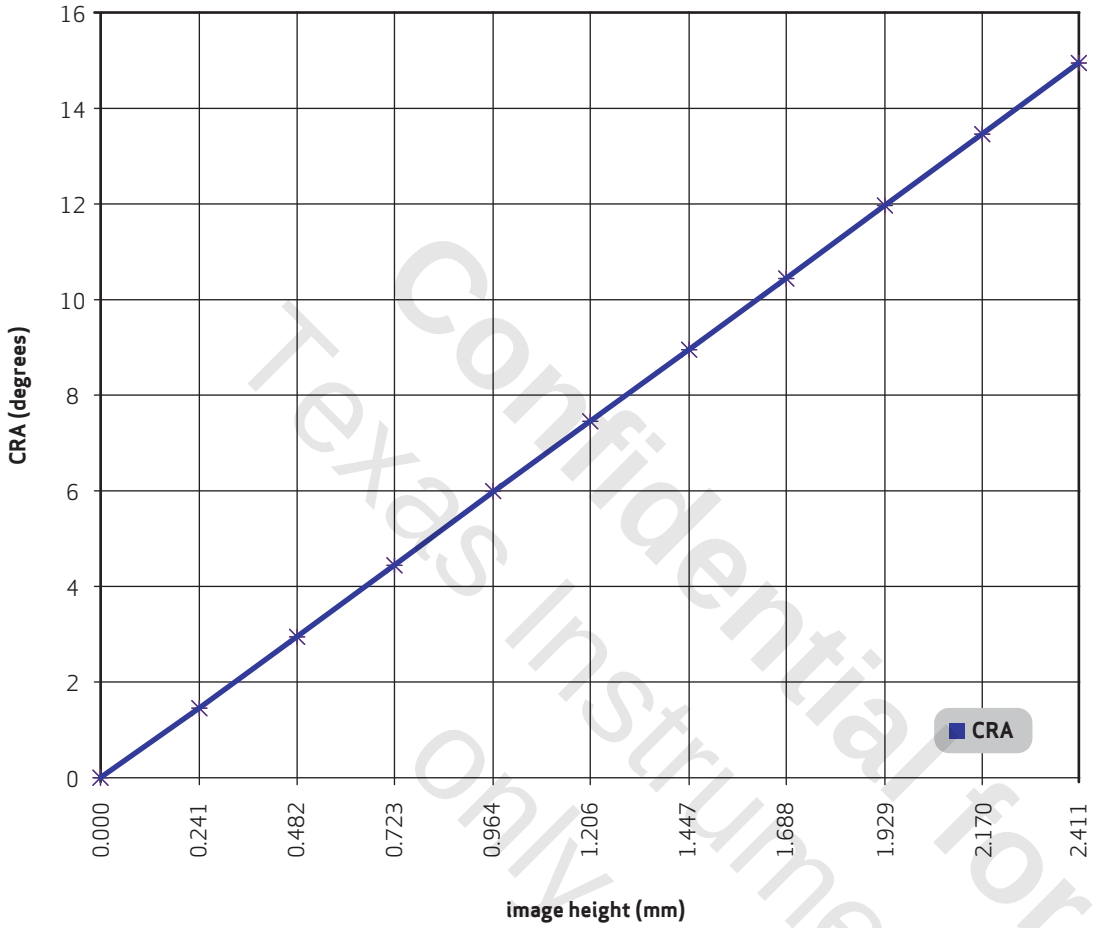


table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.00
0.10	0.241	1.50
0.20	0.482	3.00
0.30	0.723	4.50
0.40	0.964	6.00

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.50	1.206	7.50
0.60	1.447	9.00
0.70	1.688	10.50
0.80	1.929	12.00
0.90	2.170	13.50
1.00	2.411	15.00

appendix A register table

A.1 module name and address range

table A-1 module name and address range

module name	address range
DIGITAL CORE	0x3000~0x3021
ANALOG CONTROL	0x3030~0x3050
TEMPERATURE SENSOR	0x3060~0x3069
ASIL CONTROL	0x3080~0x3094
OUTPUT TIMING CONTROL	0x30A0~0x311F
BLC CONTROL	0x3140~0x318F
FORMAT CONTROL	0x3190~0x31AF
DVP CONTROL	0x31B0~0x31CF
MIPI CONTROL	0x31D0~0x321C
ISP CONTROL	0x3250~0x3258
LENC CONTROL	0x3330~0x334E
WB GAIN CONTROL	0x3360~0x339B
OTP DPC CONTROL	0x33B0~0x33CB
DPC CONTROL	0x33E0~0x3434
WINDOW CONTROL	0x3440~0x344C
GROUP HOLD CONTROL	0x3460~0x346D
IO CONTROL	0x3480~0x3491
OTP CONTROL	0x34A0~0x34B6
SCCB CONTROL	0x7FF0~0x7FF7

A.2 device control registers

table A-2 provides a description of the device control registers contained in the OV9716. The 8-bit SCCB slave device address is defined by voltage level of GPIO1 at power up: "6C" by default or defined by 0x300C when GPIO1 has a pull-down resistor; "20" when GPIO1 has a pull-up resistor, which is hard coded and cannot be changed.

table A-2 sensor control registers (sheet 1 of 54)

address	register name	default value	R/W	description
0x3000	SCLK_PLL_PRE	0x05	RW	SCLK PLL Pre Divider
0x3001	SCLK_PLL_MULT	0x60	RW	SCLK PLL Multiplier VCO Frequency Multiplier is sclk_pll_mult+3
0x3002	SCLK_PLL_POST	0x03	RW	SCLK PLL Post Divider (1-16)
0x3003	SCLK_PLL_CONFIG	0x01	RW	Bit[7:6]: lock_precision Lock detector precision resolution setting Bit[5:4]: lock_cntref Lock detector counter setting Bit[3]: fastlock_disable 0: Enable fast locking 1: Disable fast locking Bit[2:0]: Cp Charge pump current
0x3004	PCLK_PLL_PRE	0x06	RW	PCLK PLL Pre Divider
0x3005	PCLK_PLL_PDIV	0x7B	RW	PCLK PLL Core Loop Div 1 (1-256)
0x3006	PCLK_PLL_SDIV	0x00	RW	PCLK PLL Core Loop Div 2
0x3007	PCLK_PLL_POST	0x07	RW	PCLK PLL Post Divider (1-16)
0x3008	PCLK_PLL_CTRL1	0x01	RW	PCLK and SCLK PLL Control 1 Bit[7:6]: Not used Bit[5]: sclk_pll_bypass Bypass PLL2 clock within PLL Bit[4]: sclk_pll_enable Enable PLL2 (SCLK) Bit[3]: Not used Bit[2]: pclk_pll_bypass Bypass PLL1 clock within PLL Bit[1]: pclk_pll_mipi_div Divide frequency to MIPI by 2 Bit[0]: pclk_pll_enable Enable PLL1 (PCLK)

table A-2 sensor control registers (sheet 2 of 54)

address	register name	default value	R/W	description
0x3009	PCLK_PLL_CTRL2	0x00	RW	PCLK PLL Control 2 Bit[7]: Not used Bit[6:5]: ssc_cntstep Select SSC counter step number Bit[4:2]: ssc_cntck Set SSC counter frequency Bit[1]: ssc_en Enable SSC mode Bit[0]: frac_en Enable fractional mode
0x300A	CHIP_ID_H	0x97	R	Chip ID
0x300B	CHIP_ID_L	0x16	R	Chip ID
0x300C	SCCB_ID	0x6C	RW	Bit[7:1]: SCCB_id_n Bit[0]: SCCB_id_sel
0x300D	SUB_ID	0xE0	RW	Chip Subversion ID Set by ROM Loader
0x3010	MAN_ID_H	0x7F	R	Manufacture ID High Byte
0x3011	MAN_ID_L	0xA2	R	Manufacture ID Low Byte
0x3012	SOFTWARE_CTRL1	0x00	RW	Software Control 1 Bit[7:1]: Not used Bit[0]: sfw_stb 0: Software standby 1: Streaming
0x3013	SOFTWARE_CTRL2	0x00	RW	Software Control 2 Bit[7:1]: Not used Bit[0]: sfw_rst Software reset

table A-2 sensor control registers (sheet 3 of 54)

address	register name	default value	R/W	description
0x3014	PWUP_CTRL	0x84	RW	Bit[7]: sel_src 0: Select SCLK PLL 1: Select PCLK PLL as source for SCLK Bit[6]: sel_phase 0: No inversion of SCLK 1: Inverts phase of selected clock for SCLK Bit[5]: wdp_rom_crc_en Enable for triggering watchdog pulse if ROM loader CRC fails Bit[4]: wdp_pll_lock_en Enable for triggering watchdog pulse if PLLs are not locked Bit[3]: lock_pll_settings Locks all registers from sclk_pll_pre to pclk_pll_ctrl2 Bit[2]: use_pll_lock 0: Old method PLL lock 1: Use PLL lock from PLLs Bit[1:0]: Reserved
0x3016	POST	–	R	Power On Self Test Status Bit[7:6]: Not used Bit[5:2]: sc_state State of sensor control state machine Bit[0]: romloader_ok ROM loader finished with CRC match
0x3017	PCLK_PLL_DSM_MAX_H	0x00	RW	PCLK PLL Fractional Div[19:18] (SSC Maximum High Byte)
0x3018	PCLK_PLL_DSM_MAX_L	0x00	RW	PCLK PLL Fractional Div[17:10] (SSC Maximum Low Byte)
0x3019	PCLK_PLL_DSM_MIN_H	0x00	RW	PCLK PLL Fractional Div[9:8] (SSC Minimum High Byte)
0x301A	PCLK_PLL_DSM_MIN_L	0x00	RW	PCLK PLL Fractional Div (SSC Minimum Low Byte)

table A-2 sensor control registers (sheet 4 of 54)

address	register name	default value	R/W	description
0x301B	PCLK_PLL_CONFIG	0x01	RW	Bit[7:6]: lock_precision Lock detector precision resolution setting Bit[5:4]: lock_cntref Lock detector counter setting Bit[3]: fastlock_disable 0: Enable fast locking 1: Disable fast locking Bit[2:0]: CP Charge pump current Current = 5*(cp+1)
0x3020	FORCE_STANDBY_CNT_H	0x3E	RW	After 256*force_standby_cnt Standby will be Entered Independent of Sensor State. Setting Max Value Disables Feature, High Byte
0x3021	FORCE_STANDBY_CNT_L	0x80	RW	After 256*force_standby_cnt Standby will be Entered Independent of Sensor State. Setting Max Value Disables Feature, Low byte
0x303A	ANA_CB	0x04	RW	Bit[7:6]: Not used Bit[5]: cb_en Enable color bars Bit[4]: cb_mode 0: Do not swap color bars mid-array 1: Swap color bars mid-array (mirror rows) Bit[3]: cb_swap 0: Do not swap color bars 1: Swap color bars (mirror columns) Bit[2:0]: cb_adjust ICB current level (color bar intensity)
0x3066	TS_CTRL	0x80	RW	Bit[7]: ts_en Enable temperature sensor Bit[6]: ts_standby_en Enable temperature sensor in sw_standby Bit[5:0]: Not used
0x3067	TS_RD_H	–	R	Temperature Read Out C Degrees, Signed, Sign Bit
0x3068	TS_RD_L	–	R	Temperature Read Out C Degrees, Signed Low Byte
0x3080	WIN_ST_H	0x00	RW	Start Checking in Col Nr (2 * This Number) High Byte

table A-2 sensor control registers (sheet 5 of 54)

address	register name	default value	R/W	description
0x3081	WIN_ST_L	0x00	RW	Start Checking in Col Nr (2 * This Number) Low Byte
0x3082	WIN_END_H	0x01	RW	End checking in Col Nr (2 * This Number) High Byte
0x3083	WIN_END_L	0xEF	RW	End Checking in Col Nr (2 * This Number) High Byte
0x3084	ASIL_CTRL	0x05	RW	Bit[7]: asil_data_en Must be inverse of asil_out_on_vs at all times Bit[6]: asil_on_vs ASIL uses VS row pointer (else L row pointer) Bit[5]: asil_en_dark Enable ASIL checking for dark rows Bit[4]: asil_en Enable analog ASIL insertion and digital ASIL checking, overall Bit[3:0]: asil_pattern Defines superimposed pattern in a 2x2 pixel group, to be repeated across array
0x3085	ASIL_CTRL2	0x00	RW	Bit[7:4]: Not used Bit[3]: asil_on_hcg ASIL samples are fed out of analog core as HCG data, for debug only, turn off in normal operation Bit[2]: asil_row_delay Delay selected ASIL row pointer by 1 row Bit[1:0]: asil_again ASIL analog gain, encoding: 00: 1 01: 2 10: 4 11: 8
0x3086	DELTA_HIGH	0x10	RW	Defines Acceptance Range for Measured High Value
0x3087	DELTA_LOW	0x10	RW	Defines Acceptance Range for Measured Low Value
0x3089	N_POINTER_H	0x00	RW	N, Specifying Which Failed Pixel To Be Pointed Out by row_nr and col_nr Below High Byte
0x308A	N_POINTER_L	0x01	RW	N, Specifying Which Failed Pixel To Be Pointed Out by row_nr and col_nr Below Low Byte
0x308B	ROW_NR_H	–	R	Row Number for Nth Failed Pixel High 3 Bits

table A-2 sensor control registers (sheet 6 of 54)

address	register name	default value	R/W	description
0x308C	ROW_NR_L	–	R	Row Number for Nth Failed Pixel Low Byte
0x308D	COL_NR_H	–	R	(Column Number) Div 2, for Nth Failed Pixel High 2 Bits
0x308E	COL_NR_L	–	R	Column Number, Div 2, for Nth Failed Pixel Low Byte
0x308F	FAILED_NR_H	–	R	Number of Failed Pixel Positions High Byte
0x3090	FAILED_NR_L	–	R	Number of Failed Pixel Positions Low Byte
0x3091	HIGH_LEVEL	–	R	Measured High ASIL Level
0x3092	LOW_LEVEL	–	R	Measured Low ASIL Level
0x3093	FAILED_NR_THRE_H	0x00	RW	Number of Failed Pixels Threshold to Trigger Watchdog Pulse. Disabled if Set to FFFF, High Byte
0x3094	FAILED_NR_THRE_L	0x00	RW	Number of Failed Pixels Threshold to Trigger Watchdog Pulse. Disabled if Set to FFFF, Low Byte
0x30A0	CROP_H_ST_H	0x00	RW	Start Address Horizontal High Byte
0x30A1	CROP_H_ST_L	0x00	RW	Start Address Horizontal Low Byte
0x30A2	CROP_V_ST_H	0x00	RW	Start Address Vertical High Byte
0x30A3	CROP_V_ST_L	0x00	RW	Start Address Vertical Low Byte
0x30A4	CROP_H_END_H	0x05	RW	End Address Horizontal High Byte
0x30A5	CROP_H_END_L	0x7F	RW	End Address Horizontal Low Byte
0x30A6	CROP_V_END_H	0x03	RW	End Address Vertical High Byte
0x30A7	CROP_V_END_L	0xDF	RW	End Address Vertical Low Byte
0x30A8	ODP_H_OFFS_H	0x00	RW	Horizontal Output Offset High Byte
0x30A9	ODP_H_OFFS_L	0x00	RW	Horizontal Output Offset Low Byte
0x30AA	ODP_V_OFFS_H	0x00	RW	Vertical Output Offset High Byte
0x30AB	ODP_V_OFFS_L	0x00	RW	Vertical Output Offset Low Byte
0x30AC	HORIZONTAL_OUTPUT_SIZE_H	0x05	RW	Horizontal Output Size High Byte
0x30AD	HORIZONTAL_OUTPUT_SIZE_L	0x80	RW	Horizontal Output Size Low Byte
0x30AE	VERTICAL_OUTPUT_SIZE_H	0x03	RW	Vertical Output Size High Byte

table A-2 sensor control registers (sheet 7 of 54)

address	register name	default value	R/W	description
0x30AF	VERTICAL_OUTPUT_SIZE_L	0xE2	RW	Vertical Output Size Low Byte
0x30B0	HORIZONTAL_TOTAL_SIZE_H	0x08	RW	Horizontal Total Size (HTS) High Byte
0x30B1	HORIZONTAL_TOTAL_SIZE_L	0x0A	RW	Horizontal Total Size (HTS) Low Byte
0x30B2	VERTICAL_TOTAL_SIZE_H	0x03	RW	Vertical Total Size (VTS) High Byte
0x30B3	VERTICAL_TOTAL_SIZE_L	0xF4	RW	Vertical Total Size (VTS) Low Byte
0x30B4	EXTRA_DELAY_H	0x00	RW	Last Row Can Be Extended by This Number of Clocks (fs_delay), High Byte Auto-reset to 0 if 0x30BD[0] is set. Applied to frame N+2.
0x30B5	EXTRA_DELAY_L	0x00	RW	Last Row Can Be Extended by This Number of Clocks (fs_delay), Low Byte Auto-reset to 0 if 0x30BD[0] is set. Applied to frame N+2.
0x30B6	CEXP_DCG_H	0x00	RW	Frame DCG (HCG/LCG) Exposure (in Rows)
0x30B7	CEXP_DCG_L	0x10	RW	Frame DCG (HCG/LCG) Exposure (in Rows)
0x30B8	CEXP_VS_H	0x00	RW	Frame Very Short Exposure (in Rows)
0x30B9	CEXP_VS_L	0x02	RW	Frame Very Short Exposure (in Rows)
0x30BA	RSVD	–	–	Reserved
0x30BB	CG_AGAIN	0x00	RW	Conversion Gains and Analog Gains Bit[7]: cg_vs Very short conversion gain Bit[6]: Not used Bit[5:4]: again_vs Very short analog gain Bit[3:2]: again_lcg LCG analog gain Bit[1:0]: again_hcg HCG
0x30BC	EXTRA_VTS	0x00	RW	Delay Added to VTS (in rows) Auto-reset to 0 if 0x30BD[0] is set. Applied to frame N+2 unless 0x30BD[2] is set.

table A-2 sensor control registers (sheet 8 of 54)

address	register name	default value	R/W	description
0x30BD	SENSOR_CTRL	0x03	RW	Bit[7]: use_r_rst_num Use start value for row and frame counters Bit[6]: Not used Bit[5]: fsin_retro_mode When high, makes FSIN logic work with old timing Bit[4]: fsin_en When high, FSIN mode is enabled Bit[3]: low_power_mode When high, sensor will not read exposures that are disabled (single or 2 expo) Bit[2]: vts_nplus1 When high, VTS and extra_vts changes will be applied at frame N+1 instead of frame N+2. Note that extra_delay will still be applied at frame n+2 Bit[1]: asp_col_swap_en When high, enables swapping of ADCs Bit[0]: extra_ctrl When high, extra delays will be reset when used once
0x30BE	ROW_ADDR_CTRL	0x5C	RW	Control of Row Address State Machine Bit[7:6]: vs_samp_to_dp_delay VS sample to data path delay This is a sequencer program dependent parameter Bit[5:0]: row_first_active Array row address of first active row
0x30BF	SKIP_CTRL	0x00	RW	Bit[7:3]: Not used Bit[2]: Monochrome Monochrome readout mode Bit[1]: Vsub2 Skip 2/2 rows or 1/1 rows in monochrome mode Bit[0]: Hsub2 Skip 2/2 columns or 1/1 columns in monochrome mode

table A-2 sensor control registers (sheet 9 of 54)

address	register name	default value	R/W	description
0x30C0	READ_MODE	0x80	RW	Bit[7]: always_active_dp When high, data path will stay active also when there are no valid data to process Bit[6]: align_buf_flip Flip order of align buffer readout trigger 0: VS is last 1: L is last Bit[5:4]: multi_samp Multisampling for L 00: 1 01: 2 10: 4 11: Undefined Bit[3]: Flip Reverse row readout order Bit[2]: Mirror Reverse column readout order Bit[1]: Reserved Bit[0]: align_repeat_last_row When set, repeat last row for invalid rows when always_active_dp is set
0x30C1	READ_CTRL	0x04	RW	Bit[7:6]: Not used Bit[5:4]: multi_samp_vs Multisampling for VS 00: 1 01: 2 10: 4 11: Undefined Bit[3]: force_dcg In DCG mode, force read-out of CG to value of cg_l/cg_vs register Bit[2]: show_emb_rows Show embedded rows Bit[1:0]: Not used
0x30C5	ALU_TEST_CTRL	0x00	RW	Bit[7:2]: Not used Bit[1]: alu_mbist_mode Enable ALU MBIST, will replace data input to ALU with BIST data, same for SHR and SHS Bit[0]: Not used
0x30C6	ALU_MBIST	–	R	Bit[7:4]: Not used Bit[3:2]: memory_failed 0: VS memory failed 1: DCG memory failed Bit[1:0]: test_failed ALU MBIST failed

table A-2 sensor control registers (sheet 10 of 54)

address	register name	default value	R/W	description
0x30C7	TC_R_RST_NUM_H	0x00	RW	Manual Start Value for Row and Frame Counters in FSIN mode. Enabled by sensor_ctrl.use_r_rst_num, High byte
0x30C8	TC_R_RST_NUM_L	0x00	RW	Manual Start Value for Row and Frame Counters in FSIN Mode. Enabled by sensor_ctrl.use_r_rst_num, Low Byte
0x30C9	EXP_DCG_H	–	R	Current Frame DCG (HCG/LCG) Exposure Time (in Rows) High Byte
0x30CA	EXP_DCG_L	–	R	Current Frame DCG (HCG/LCG) Exposure Time (in Rows) Low Byte
0x30CB	EXP_VS_H	–	R	Current Frame Very Short Exposure Time (in Rows) High Byte
0x30CC	EXP_VS_L	–	R	Current Frame Very Short Exposure Time (in Rows) Low Byte
0x30CD	EXP_VS_F	–	R	Current Frame Fractional Very Short Exposure (Actual Adjusted Value)
0x30CE	VS_DP_DELAY_H	–	R	Current Frame Very Short Data Path Delay in Rows High Byte
0x30CF	VS_DP_DELAY_L	–	R	Current Frame Very Short Data Path Delay in Rows Low Byte
0x30D0	CG_AGAIN_USE	–	R	Bit[7]: cg_vs Current frame very short conversion gain Bit[6]: Not used Bit[5:4]: again_vs Current frame very short analog gain Bit[3:2]: again_lcg Current frame LCG analog gain Bit[1:0]: again_hcg Current frame HCG/linear analog gain
0x30D1	ASIL_PATTERN_CTRL	0x04	RW	Control of ASIL Pattern Overlay Bit[7:2]: Not used Bit[1]: pattern_en Enable pattern Bit[0]: pulse_en Enable pulsation of pattern
0x30D2	ASIL_PATTERN_LOW	0x00	RW	Low Pixel Value in ASIL Pattern
0x30D3	ASIL_PATTERN_HIGH	0x80	RW	High Pixel Value in ASIL pattern

table A-2 sensor control registers (sheet 11 of 54)

address	register name	default value	R/W	description
0x30D4	COL_TAG_CTRL	0x00	RW	Control of Column Tag Bit[7:4]: col_tag_width Column tagger width Bit[3:2]: Not used Bit[1]: col_tag_inv Invert column tagger Bit[0]: col_tag_en Enable column tagger
0x30D5	FCNT_3	–	R	Frame Count Byte 3
0x30D6	FCNT_2	–	R	Frame Count Byte 2
0x30D7	FCNT_1	–	R	Frame Count Byte 1
0x30D8	FCNT_0	–	R	Frame Count Byte 0
0x30FF	SEQ_CRC_H	–	R	Sequencer CRC from Last Row High Byte
0x3100	SEQ_CRC_L	–	R	Sequencer CRC from Last Row Low Byte
0x3101	SEQ_CRC_EXPECT_H	0x00	RW	Expected Sequencer CRC High byte
0x3102	SEQ_CRC_EXPECT_L	0x00	RW	Expected Sequencer CRC Low Byte
0x3103	SEQ_STATUS	0x00	RW	Bit[7:4]: Not used Bit[3]: wdp_crc_en Enables seq_crc_fail to contribute to watch dog pulse generation Bit[2]: wdp_timing_en Enables seq_timing_fail to contribute to watch dog pulse generation Bit[1]: seq_crc_fail Status bit is set to one if sequencer CRC does not match (write 0 to reset) Bit[0]: seq_timing_fail Status bit is set to one if sequencer did not finish within HTS
0x310E	LOCK_TC	0x00	RW	Lock Control On Timing Control Registers Bit[7:5]: Not used Bit[4]: lock_read_mode Lock read_mode register Bit[3]: lock_vts Lock VTS registers Bit[2]: lock_hts Lock HTS registers Bit[1]: lock_h_crop Lock h_crop registers Bit[0]: lock_v_crop Lock v_crop registers

table A-2 sensor control registers (sheet 12 of 54)

address	register name	default value	R/W	description
0x3140	BLC_CTRL	0x02	RW	Bit[7]: Not used Bit[6:4]: blc_override_en Use manual BLC values from blc_override_* registers. Separate enable for HCG (Bit[4]), LCG (Bit[5]) and VS (Bit[6]) exposures Bit[3]: blc_cont_update_mode Enable BLC recalculation on every frame Bit[1]: blc_dither_en Enable dithering on unused sub-LSBs of incoming data Bit[0]: show_dark_rows Show dark rows in image
0x314C	BLC_OVERRIDE_HCG_H	0x00	RW	Manual BLC Override Value for HCG Exposure High Byte
0x314D	BLC_OVERRIDE_HCG_L	0x00	RW	Manual BLC Override Value for HCG Exposure Low Byte
0x314E	BLC_OVERRIDE_LCG_H	0x00	RW	Manual BLC Override Value for LCG Exposure High Byte
0x314F	BLC_OVERRIDE_LCG_L	0x00	RW	Manual BLC Override Value for LCG Exposure Low Byte
0x3150	BLC_OVERRIDE_VS_H	0x00	RW	Manual BLC Override Value for VS Exposure High Byte
0x3151	BLC_OVERRIDE_VS_L	0x00	RW	Manual BLC Override Value for VS Exposure Low Byte

table A-2 sensor control registers (sheet 13 of 54)

address	register name	default value	R/W	description
0x3152	FRAME_FILTER_CTRL	0x04	RW	Frame Filter Control Bit[7:3]: Not used Bit[2]: frfilt_old_value_select Select 'old' dark level value to be used in alpha filter 0: Official 'last dark level' 1: Stored filter output from previous frame Bit[1]: frfilt_hard_thres_mux_select Input to delta-computation in front of hard threshold comparator is dark level value 0: After alpha filter 1: Before alpha filter Bit[0]: frfilt_main_thres_mux_select Input to delta-computation in front of main threshold comparator is dark level value 0: After alpha filter 1: Before alpha filter
0x315F	AB_CTRL	0x00	RW	Controls AB Mode Operation (Bit[0] Must Be Set and Bit[1] Must Be Toggled, 0: A Frame, 1: B Frame) Bit[7:6]: blc_raw_sel 00: HCG 01: LCG 10: VS 11: Not used Bit[5:2]: Not used Bit[1]: Bframe Selects between A (0) and B (1) frames Bit[0]: ab_mode Enable AB mode
0x3160	BLC_MAX_CORRECTION_H	0x0F	RW	Maximum Value of BLC Correction High Byte
0x3161	BLC_MAX_CORRECTION_L	0xFF	RW	Maximum Value of BLC Correction Low Byte
0x3162	DIG_GAIN_HCG_H	0x01	RW	Digital Gain for HCG (Format 6.8) High Byte
0x3163	DIG_GAIN_HCG_L	0x00	RW	Digital Gain for HCG (Format 6.8) Low Byte
0x3164	DIG_GAIN_LCG_H	0x01	RW	Digital Gain for LCG (Format 6.8) High Byte
0x3165	DIG_GAIN_LCG_L	0x00	RW	Digital Gain for LCG (Format 6.8) Low Byte
0x3166	DIG_GAIN_VS_H	0x01	RW	Digital Gain for VS (Format 6.8) High Byte
0x3167	DIG_GAIN_VS_L	0x00	RW	Digital Gain for VS (Format 6.8) Low Byte

table A-2 sensor control registers (sheet 14 of 54)

address	register name	default value	R/W	description
0x3168	BLC_TARGET_HCG_H	0x00	RW	Black Level Target HCG Exposure High Byte
0x3169	BLC_TARGET_HCG_L	0x40	RW	Black Level Target HCG Exposure Low Byte
0x316A	BLC_TARGET_LCG_H	0x00	RW	Black Level Target LCG Exposure High Byte
0x316B	BLC_TARGET_LCG_L	0x40	RW	Black Level Target LCG Exposure Low Byte
0x316C	BLC_TARGET_VS_H	0x00	RW	Black Level Target VS Exposure High Byte
0x316D	BLC_TARGET_VS_L	0x40	RW	Black Level Target VS Exposure Low Byte
0x316E	DIG_GAIN_FS2_HCG_H	–	R	Readback of Frame Synchronized Digital Gain for HCG Exposure High Byte
0x316F	DIG_GAIN_FS2_HCG_L	–	R	Readback of Frame Synchronized Digital Gain for HCG Exposure Low Byte
0x3170	DIG_GAIN_FS2_LCG_H	–	R	Readback of Frame Synchronized Digital Gain for LCG Exposure High Byte
0x3171	DIG_GAIN_FS2_LCG_L	–	R	Readback of Frame Synchronized Digital Gain for LCG Exposure Low Byte
0x3172	DIG_GAIN_FS2_VS_H	–	R	Readback of Frame Synchronized Digital Gain for VS Exposure High Byte
0x3173	DIG_GAIN_FS2_VS_L	–	R	Readback of Frame Synchronized Digital Gain for VS Exposure Low Byte
0x3174	BLC_TARGET_FS2_HCG_H	–	R	Readback of Black Level Target HCG Exposure High Byte
0x3175	BLC_TARGET_FS2_HCG_L	–	R	Readback of Black Level Target HCG Exposure Low Byte
0x3176	BLC_TARGET_FS2_LCG_H	–	R	Readback of Black Level Target LCG Exposure High Byte
0x3177	BLC_TARGET_FS2_LCG_L	–	R	Readback of Black Level Target LCG Exposure Low Byte
0x3178	BLC_TARGET_FS2_VS_H	–	R	Readback of Black Level Target VS Exposure High Byte
0x3179	BLC_TARGET_FS2_VS_L	–	R	Readback of Black Level Target VS Exposure Low Byte
0x317A	DARK_CURRENT_HCG_H	–	R	Dark Current Compensation for HCG Exposure (Signed) High Byte
0x317B	DARK_CURRENT_HCG_L	–	R	Dark Current Compensation for HCG Exposure (3 Sub-LSBs) Low Byte
0x317C	DARK_CURRENT_LCG_H	–	R	Dark Current Compensation for LCG Exposure (Signed) High Byte

table A-2 sensor control registers (sheet 15 of 54)

address	register name	default value	R/W	description
0x317D	DARK_CURRENT_LCG_L	–	R	Dark Current Compensation for LCG Exposure (3 Sub-LSBs) Low Byte
0x317E	DARK_CURRENT_VS_H	–	R	Dark Current Compensation for VS Exposure (Signed) High Byte
0x317F	DARK_CURRENT_VS_L	–	R	Dark Current Compensation for VS Exposure (3 Sub-LSBs) Low Byte
0x3180	ROW_AVERAGE_HCG_H	–	R	Row Average (Accumulator Value) for HCG Exposure (Signed) High Byte
0x3181	ROW_AVERAGE_HCG_L	–	R	Row Average (Accumulator Value) for HCG Exposure (3 Sub-LSBs) Low Byte
0x3182	ROW_AVERAGE_LCG_H	–	R	Row Average (Accumulator Value) for LCG Exposure (Signed) High Byte
0x3183	ROW_AVERAGE_LCG_L	–	R	Row Average (Accumulator Value) for LCG Exposure (3 Sub-LSBs) Low Byte
0x3184	ROW_AVERAGE_VS_H	–	R	Row Average (Accumulator Value) for VS Exposure (Signed) High Byte
0x3185	ROW_AVERAGE_VS_L	–	R	Row Average (Accumulator Value) for VS Exposure (3 Sub-LSBs) Low Byte
0x318F	BFRAME_FS2	–	R	Readback of Frame Synchronized Bframe Bit from ab_ctrl register
0x3190	INTERFACE_CTRL0	0x07	RW	Bit[7]: channel_cfg Channel configuration Bit[6]: Linear mode conversion gain 0: LCG 1: HCG Bit[5]: mode_10b Output 10-bit data, only supported by some modes Bit[4]: no_comp When high, single 12 bits data are sent without compression Bit[3]: lin_enable Fast linear mode enable (not supported, logic is kept, but not verified) Bit[2]: vs_enable Staggered VS mode enable Bit[1:0]: data_width 00: Not used 01: 2x12 10: 12 combined 11: 16 combined

table A-2 sensor control registers (sheet 16 of 54)

address	register name	default value	R/W	description
0x3191	INTERFACE_CTRL1	0xB9	RW	Bit[7]: img_size_vfifo_sel Select automatically calculated image size for MIPI output Bit[6]: mask_vs_sof Mask VS SOF Only use when both DCG channel and VS channel have same channel ID Bit[5]: hts_pclk_man_en HTS PCLK manual override when SCLK to PCLK ratio does not fit any preprogrammed mode Bit[4:1]: Not used Bit[0]: if_mode 0: DVP 1: MIPI
0x3193	HTS_PCLK_MAN_H	0x08	RW	HTS in PCLKs, Manual Override Value, for DVP Only High Byte
0x3194	HTS_PCLK_MAN_L	0x0A	RW	HTS in PCLKs, Manual Override Value, for DVP Only Low Byte
0x3195	VFIFO_READ_LEVEL	0x2E	RW	When to Start Reading from VFIFO SRAMs
0x3196	FO_WAIT_TIME_H	0x00	RW	Cool-down Time in PCLKS After Streaming Session Before Next Streaming Session High Byte
0x3197	FO_WAIT_TIME_L	0x00	RW	Cool-down Time in PCLKS After Streaming Session Before Next Streaming Session Low Byte
0x31A0	MIPI_FORMAT	0x2C	RW	Bit[7]: mipi_byte_switch MIPI byte switch in 16-bit mode Bit[6]: Not used Bit[5:4]: mipi_vch_id_third Virtual channel ID for third channel, only used on VS Bit[3:2]: mipi_vch_id_sec Virtual channel ID for secondary DCG channel, not used in linear mode Bit[1:0]: mipi_vch_id_main Virtual channel ID for first DCG channel or in linear mode
0x31A1	MIPI_DUMMY_DATA	0x55	RW	Dummy Data to Output During Dummy Rows (MSB-aligned to 12-bit)

table A-2 sensor control registers (sheet 17 of 54)

address	register name	default value	R/W	description
0x31A2	FORMAT_SETTINGS	0x00	RW	Bit[7]: format_sel_vs Output VS exposure when in one exposure mode Bit[6]: format_sel_one_exp Mode for easy output of one exposure and switch between 3 exposures using format_sel and format_sel_vs, used to get regular linear mode Bit[5]: disable_arbiter Disable arbiter (always give VFIFO access to FI1) Bit[4:3]: dvp_16b_opt 00: Advanced 16-bit DVP packing 01: Not used 10: 2-cycle packing option A (MSB) 11: 2-cycle packing option B (12-bit) Bit[2]: reset_crc_error_cnt Write to reset CRC error count, Auto-reset Bit[1:0]: flag_2x12 Manual flag settings for 2x12 mode
0x31A3	VFIFO_MANUAL_ OVERRIDE	0x00	RW	Manual Override of VFIFO Functions Bit[7:6]: vfifo_lane_fill_inc_man Manual lane fill inc Bit[5:4]: vfifo_lane_fill_cap_man Manual lane fill cap Bit[3]: vfifo_lane_fill_man Use manually set lane fill Bit[2:1]: vfifo_inp_data_width_man Manual input data width for VFIFO Bit[0]: vfifo_inp_data_width_man_en Use manually set input data width for VFIFO

table A-2 sensor control registers (sheet 18 of 54)

address	register name	default value	R/W	description
0x31A4	VFIFO_STATUS	–	R	Bit[7:6]: Not used Bit[5]: fo_q_error_ch2 FO overflow (data is not getting out from VFIFO) Bit[4]: fo_q_empty_ch2 FO is empty (it should not always be 1) Bit[3]: fo_q_error_ch1 FO overflow (data is not getting out from VFIFO) Bit[2]: fo_q_empty_ch1 FO is empty (it should not always be 1) Bit[1]: fo_q_error_ch0 FO overflow (data is not getting out from VFIFO) Bit[0]: fo_q_empty_ch0 FO is empty (it should not always be 1)
0x31A5	VFIFO_CRC_ERROR_COUNT	–	R	VFIFO CRC Error Count, Number of Lines That Failed CRC Check
0x31A6	VFIFO_CRC_ERROR_THRE	0x00	RW	VFIFO CRC Error Count Threshold to Trigger Watchdog Pulse. Disabled if 0xFF

table A-2 sensor control registers (sheet 19 of 54)

address	register name	default value	R/W	description
0x31A7	VFIFO_CTRL	0xD8	RW	Bit[7]: vfifo_idle_ro Emulate VFIFO read-out in unalign MIPI-mode when no data is present. VFIFO does not go idle (more power is used), but power consumption is more even over a frame time. Bit[6]: discard_idle_ro_int Do not output dummy data from VFIFO. All dummy data is discarded internally in VFIFO. Dummy data is only useful if we want to avoid banding or if user does not have proper handling for virtual channels. Bit[5]: discard_idle_ro_at_io Output dummy data from VFIFO, but discards it right before pads instead. This is optimal solution to avoid banding. Bit[4]: vfifo_fake_ro Emulate VFIFO read-out in unalign MIPI-mode for missing exposure. VFIFO does not go idle (more power is used), but MIPI output timing is more even. Required in 16+12-bit MIPI-mode Bit[3]: discard_fake_ro_int Do not output dummy data from VFIFO. All dummy data is discarded internally in VFIFO. Should always stay on unless always_active_dp is used. Dummy data is only useful when avoiding banding or user does not have proper handling for virtual channels. Bit[2]: discard_fake_ro_at_io Output dummy data from VFIFO, but discards it right before pads instead. This is optimal solution to avoid banding. Bit[1]: Not used Bit[0]: fo_q_error_wdp_en Enable for triggering watchdog pulse on fo_q_error

table A-2 sensor control registers (sheet 20 of 54)

address	register name	default value	R/W	description
0x31A8	VFIFO_CTRL2	0x02	RW	Bit[7]: dvp_allow_dummy When set dummy data will be output on DVP pads for inactive exposures. When not set inactive exposures will output 0s. Bit[6]: fo_sync_mode 0: Sync on any/every vfifo_rd_start 1: Sync on first vfifo_rd_start after sof_l (FS) Bit[5]: fo_sync_man Enable manual sync mode with trigger (FS) Bit[4]: fo_sync_trigger Trigger resync of fo_timer. Use fo_sync_mode to select if it should be resync'd immediately or after first SOF_L, auto-reset. Bit[3]: vfifo_fo_no_sof_timer Do not use timer for SOF. vfifo_fo_queue_en must be enabled. Bit[2]: vfifo_fo_instant_sof Do not queue SOF. Send them directly, not permitted in MIPI mode. Bit[1]: vfifo_fo_priority_sof Drop next queued data read when SOF has been queued. Use only when discard_fake_ro_at_io and always_active_dp & if_mode == MIPI_MODE. Ignored if always_active_dp = 0. Bit[0]: vfifo_fo_queue_en Enable queueing of read-outs in VFIFO_FO. This will increase bandwidth, but HBlank is not guaranteed to be consistent.
0x31B0	VSYNC_WIDTH_LINE_H	0x00	RW	VSYNC Width by Line Number High Byte
0x31B1	VSYNC_WIDTH_LINE_L	0x00	RW	VSYNC Width by Line Number Low Byte
0x31B2	VSYNC_WIDTH_PIXEL_H	0x02	RW	VSYNC Width by Pixel Number High Byte
0x31B3	VSYNC_WIDTH_PIXEL_L	0x00	RW	VSYNC Width by Pixel Number Low Byte
0x31B4	VSYNC_DELAY_H	0x00	RW	VSYNC Delay Count High Byte
0x31B5	VSYNC_DELAY_M	0x01	RW	VSYNC Delay Count Middle Byte
0x31B6	VSYNC_DELAY_L	0x00	RW	VSYNC Delay Count Low Byte

table A-2 sensor control registers (sheet 21 of 54)

address	register name	default value	R/W	description
0x31B7	POLARITY_CTRL	0x00	RW	Polarity Control Register Bit[7]: Not used Bit[6]: bit_reverse_enable Invert output bits Bit[5:3]: Not used Bit[2]: href_polarity 0: Active high 1: Active low Bit[1]: vsync_polarity 0: Active high 1: Active low Bit[0]: pclk_polarity Output inverted PCLK
0x31B8	TEST_ORDER	0x00	RW	Test Pattern Mode Bit[7]: Not used Bit[6:4]: Reserved Bit[3]: test_mode When set, only change data every other clock Bit[2]: test_bit10 Enable 10-bit test Bit[1]: test_bit8 Enable 8-bit test Bit[0]: test_enable Enable test
0x31B9	BYP_SELECT	0x00	RW	Bypass Select Bit[7:6]: Not used Bit[5]: data_bit_shift Used in test mode to select between bit swap methods when using 16 bits Bit[4:0]: Not used
0x31BA	R_FIFO	0x00	RW	Top Sync FIFO Control Bit[7:2]: Not used Bit[1]: dvp_sync_pclk_pol Invert output PCLK within DVP_SYNC module Bit[0]: dvp_sync_pll_pclk_inv Invert input PLL PCLK within DVP_SYNC module
0x31E3	MIPI_CLK_PERIOD1	0x00	RW	Clock Period of mipi_clk Used to Calculate Timing Parameters of MIPI TX (Low 2 Bits, Fraction) User May Update This Register When mipi_clk Clock Cycle is Changed. mipi_clk Default is 125.0 MHz

table A-2 sensor control registers (sheet 22 of 54)

address	register name	default value	R/W	description
0x31E4	MIPI_CLK_PERIOD2	0x08	RW	Clock Period of mipi_clk Used to Calculate Timing Parameters of MIPI TX (High 8 Bits, Integer) Default Value: 8.00ns. User May Update This Register When mipi_clk Clock Cycle is Changed. mipi_clk Default is 125.0 MHz
0x31E5	MIPI_LANE_CTRL0	0x82	RW	Data/clock Lane Control Register Bit[7]: ext_timing Finish lane transfer long packet data exactly 0: Send any dummy data in data lane when image line byte number (add 2 CRC byte) can not be divided by lane number. That means, there will be one dummy byte in some data lanes 1: Do not send any dummy data in data lane. That means trail data will behind image data in each data lane. Bit[6]: clk_data_chg Clock lane data change from 2'b01 to 2'b10 Bit[5]: dis_clk_lane (active high) Disable clock lane Bit[4]: line_sync_en Insert LS/LE in MIPI TX stream if this bit is set Bit[3]: frame_cnt_zero_c1 MIPI TX channel 1 will keep frame counter zero if this bit is set Bit[2]: frame_cnt_zero_c0 MIPI TX channel 0 will keep frame counter zero if this bit is set Bit[1]: gate_clk_en2 (active high) Gate clock of clock lane when frame blanking time Bit[0]: gate_clk_en1 (active high) Gate clock of clock lane when line/frame blanking time mipi_lpkt_man 0x00 MIPI TX long packet manual mode, Default value: 8'h00

table A-2 sensor control registers (sheet 23 of 54)

address	register name	default value	R/W	description
0x31E6	MIPI_LPKT_MAN	0x00	RW	MIPI TX Long Packet Manual Mode Bit[7]: Not used Bit[6]: lpkt_man_en Long packet manual input Bit[5:0]: dt_manual Manual data type
0x31E7	MIPI_DI0	0x30	RW	MIPI Data Identifier Register 0 (RAW16) Bit[7:6]: vc_num0 Virtual channel ID for data path 0 Bit[5:0]: img_dt0 Data type for data path 0
0x31E8	MIPI_DI1	0x6C	RW	MIPI Data Identifier Register 1 (RAW12) Bit[7:6]: vc_num1 Virtual channel ID for data path 0 Bit[5:0]: img_dt1 Data type for data path 0
0x31E9	MIPI_DI2	0xAC	RW	MIPI Data Identifier Register 2 (RAW12) Bit[7:6]: vc_num2 Virtual channel ID for data path 0 Bit[5:0]: img_dt2 Data type for data path 0
0x31EA	MIPI_DI3	0xEC	RW	MIPI Data Identifier Register 3 (RAW12) Bit[7:6]: vc_num3 Virtual channel ID for data path 0 Bit[5:0]: img_dt3 Data type for data path 0
0x31EB	MIPI_EMB	0x3F	RW	MIPI Embedded Data Identifier Bit[7]: Not used Bit[6]: use_emb_data_type Use embedded data type for embedded data rows Bit[5:0]: emb_dt Data type for embedded data
0x31EC	MIPI_IMG_WIDTHH0	0x0B	RW	Bit[7:0]: img_width[15:8] Channel 0 image width high byte
0x31ED	MIPI_IMG_WIDTHL0	0x00	RW	Bit[7:0]: img_width[7:0] Channel 0 image width low byte
0x31EE	MIPI_IMG_HEIGHTH0	0x03	RW	Bit[7:0]: img_height[15:8] Channel 0 image height high byte
0x31EF	MIPI_IMG_HEIGHTL0	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 0 image height low byte
0x31F0	MIPI_IMG_WIDTHH1	0x05	RW	Bit[7:0]: img_width[15:8] Channel 1 image width high byte

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address	register name	default value	R/W	description
0x31F1	MIPI_IMG_WIDTHL1	0x80	RW	Bit[7:0]: img_width[7:0] Channel 1 image width low byte
0x31F2	MIPI_IMG_HEIGHTH1	0x03	RW	Bit[7:0]: img_height[15:8] Channel 1 image height high byte
0x31F3	MIPI_IMG_HEIGHTL1	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 1 image height low byte
0x31F4	MIPI_IMG_WIDTHH2	0x05	RW	Bit[7:0]: img_width[15:8] Channel 2 image width high byte
0x31F5	MIPI_IMG_WIDTHL2	0x80	RW	Bit[7:0]: img_width[7:0] Channel 2 image width low byte
0x31F6	MIPI_IMG_HEIGHTH2	0x03	RW	Bit[7:0]: img_height[15:8] Channel 2 image height high byte
0x31F7	MIPI_IMG_HEIGHTL2	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 2 image height low byte
0x31F8	MIPI_IMG_WIDTHH3	0x05	RW	Bit[7:0]: img_width[15:8] Channel 3 image width high byte
0x31F9	MIPI_IMG_WIDTHL3	0x80	RW	Bit[7:0]: img_width[7:0] Channel 3 image width low byte
0x31FA	MIPI_IMG_HEIGHTH3	0x03	RW	Bit[7:0]: img_height[15:8] Channel 3 image height high byte
0x31FB	MIPI_IMG_HEIGHTL3	0xE0	RW	Bit[7:0]: img_height[7:0] Channel 3 image height low byte
0x31FC	MIPI_STATUS	–	R	MIPI Status Register Bit[7:2]: Not used Bit[1]: mipi_ph_done MIPI has transferred long packet header data. User can modify data type. Bit[0]: mipi_busy MIPI is transmitting data if this bit is assert

table A-2 sensor control registers (sheet 25 of 54)

address	register name	default value	R/W	description
0x31FD	MIPI_LANE_CTRL1	0xCB	RW	MIPI Data Lane Control Register 1 Bit[7]: hs_zero_sync_en 0: Send hs_en one cycle ahead of hs_zero state 1: Send hs_en sync with hs_zero state Bit[6]: sof_send_fs Send FS packet after MIPI received SOF 0: Send FS packet when VFIFO data is ready 1: Send FS packet when MIPI received SOF Bit[5]: chksum_exchg Long packet checksum byte exchange enable 0: Chksum = CRC[15:0] 1: Chksum = (CRC[7:0], CRC[15:8]) Bit[4]: Reserved Bit[3]: lp_state Low power state when data lane is idle 0: Low power signal for each data lane may be controlled by lane_en. That means, if related lane_en is active, low power state of this data lane will stay 1 as idle. Other non-active lanes will stay 0 1: lp_p or lp_n will stay 1 if current data lane is not active Bit[2]: pclk_inv_en (active high) PCLK inverse enable (output to PHY) Bit[1]: gen_fe_en1 Force to generate frame end short packet in channel 1 when MIPI TX has transmitted one line if VFIFO of this channel is overflow Bit[0]: gen_fe_en0 Force to generate frame end short packet in channel 0 when MIPI TX has transmitted one line if VFIFO of this channel is overflow

table A-2 sensor control registers (sheet 26 of 54)

address	register name	default value	R/W	description
0x31FE	MIPI_LANE_CTRL2	0x0F	RW	MIPI Data Lane Control Register 2 Bit[7]: d4_inv_en Data lane 4 inverse enable Bit[6]: d3_inv_en Data lane 3 inverse enable Bit[5]: d2_inv_en Data lane 2 inverse enable Bit[4]: d1_inv_en Data lane 1 inverse enable Bit[3]: lane4_en Data lane 4 enable Bit[2]: lane3_en Data lane 3 enable Bit[1]: lane2_en Data lane 2 enable Bit[0]: lane1_en Data lane 1 enable

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address	register name	default value	R/W	description
0x31FF	MIPI_LANE_CTRL3	0x03	RW	MIPI Data Lane Control Register 3 Bit[7]: ch3_crop_en Channel 3 crop enable 0: Channel 3 crop disable 1: Channel 3 crop enable Bit[6]: ch2_crop_en Channel 2 crop enable 0: Channel 2 crop disable 1: Channel 2 crop enable Bit[5]: ch1_crop_en Channel 1 crop enable 0: Channel 1 crop disable 1: Channel 1 crop enable Bit[4]: ch0_crop_en Channel 0 crop enable 0: Channel 0 crop disable 1: Channel 0 crop enable Bit[3]: fcnt_zero_c3 MIPI TX channel 3 will keep frame counter zero if this bit is set Bit[2]: fcnt_zero_c2 MIPI TX channel 2 will keep frame counter zero if this bit is set Bit[1]: gen_fe_en3 Force to generate frame end short packet in Channel 3 when MIPI TX has transmitted one line if VFIFO of this channel is overflow Bit[0]: gen_fe_en2 Force to generate frame end short packet in Channel 2 when MIPI TX has transmitted one line if VFIFO of this channel is overflow

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address	register name	default value	R/W	description
0x3200	MIPI_TEST_MODE	0x00	RW	MIPI TX Test Mode Bit[7:6]: Not used Bit[5]: lp_n_man_data Output manual lower power data in MIPI TX test mode Bit[4]: lp_p_man_data Output manual lower power data in MIPI TX test mode Bit[3]: lp_man_en Output manual low power data enable in low power test mode and de-assert high speed signal (hs_en or valid) Bit[2]: hs_man_en Manual test data will output to PHY when this bit is set and MIPI TX in high speed test mode Bit[1]: test_mode 0: Test start point sync by mipi_test 1: Test start point sync by MIPI RX prbs_en Bit[0]: mipi_test (active high) Test MIPI TX and RX PHY
0x3201	MANUAL_TEST_DATA	0xFF	RW	Manual Test Data for MIPI PHY
0x3202	MIPI_TEST_CFG	0x00	RW	MIPI Test Configuration Bit[7:2]: Not used Bit[1:0]: rx_prbs_en Enable MIPI PHY test including RX PHY and TX PHY
0x3203	MAX_FRAME_CNTH0	0xFF	RW	Maximum Frame Counter of Channel 0 High Byte
0x3204	MAX_FRAME_CNTL0	0xFF	RW	Maximum Frame Counter of Channel 0 Low Byte
0x3205	MAX_FRAME_CNTH1	0xFF	RW	Maximum Frame Counter of Channel 1 High Byte
0x3206	MAX_FRAME_CNTL1	0xFF	RW	Maximum Frame Counter of Channel 1 Low Byte
0x3207	MAX_FRAME_CNTH2	0xFF	RW	Maximum Frame Counter of Channel 2 High Byte
0x3208	MAX_FRAME_CNTL2	0xFF	RW	Maximum Frame Counter of Channel 2 Low Byte
0x3209	MAX_FRAME_CNTH3	0xFF	RW	Maximum Frame Counter of Channel 3 High Byte

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address	register name	default value	R/W	description
0x320A	MAX_FRAME_CNTL3	0xFF	RW	Maximum Frame Counter of Channel 3 Low Byte
0x320B	YUV422_12B_DT	0x1B	RW	YUV422_12b Data Type
0x320C	YUV422_10B_DT	0x1F	RW	YUV422_10b Data Type
0x320D	YUV422_8B_DT	0x1E	RW	YUV422_8b Data Type
0x320E	RAW16_DT	0x30	RW	RAW16 Data Type
0x320F	RAW14_DT	0x2D	RW	RAW14 Data Type
0x3210	RAW12_DT	0x2C	RW	RAW12 Data Type
0x3211	RAW10_DT	0x2B	RW	RAW10 Data Type
0x3212	RAW8_DT	0x2A	RW	RAW8 Data Type
0x3213	RGB888_DT	0x24	RW	RGB888 Data Type
0x3214	RGB565_DT	0x22	RW	RGB565 Data Type

table A-2 sensor control registers (sheet 30 of 54)

address	register name	default value	R/W	description
0x3215	DAT_SEQ_CTRL	0x00	RW	Data Sequence Control Bit[7:5]: total_seq RGB sequence 000: BGR 001: BRG 010: GBR 011: GRB 100: RGB 101: RBG Bit[4:3]: high_half_seq Quarter sequence Used to adjust each 12-bits data sequence 00: Data[11:0] 01: (Data[9:0], data[11:10]) 10: (Data[7:0], data[11:8]) 11: Data[11:0] Bit[2]: low_half_seq Low half sequence Used to adjust low 24-bits data sequence 0: Data[23:0] 1: (Data[11:0], data[23:12]) Bit[1]: quarter_seq High half sequence Used to adjust low 24-bits data sequence 0: Data[47:24] 1: (Data[35:24], data[47:36]) Bit[0]: rgb_seq Total sequence 0: Data[47:0] 1: (Data[11:0], data[23:12], data[35:24], data[47:36])
0x3216	LP_DELAY	0x04	RW	LP00~LP11 Delay Cycle When hs_zero Sync Enable
0x3217	MIPI_DATA_TAG0	0x30	RW	Data_ID Tag Transmitted in Virtual Channel 0 for Supporting "Same Image Data Transmit in Different Virtual Channel with Different Data_ID Tag" Case
0x3218	MIPI_DATA_TAG1	0x6C	RW	Data_ID Tag Transmitted In Virtual Channel 1 for Supporting "Same Image Data Transmit in Different Virtual Channel with Different Data_ID Tag" Case

table A-2 sensor control registers (sheet 31 of 54)

address	register name	default value	R/W	description
0x3219	MIPI_DATA_TAG2	0xAC	RW	Data_ID Tag Transmitted in Virtual Channel 2 for Supporting "Same Image Data Transmit in Different Virtual Channel with Different Data_ID Tag" Case
0x321A	MIPI_DATA_TAG3	0xEC	RW	Data_ID Tag Transmitted in Virtual Channel 3 for Supporting "Same Image Data Transmit in Different Virtual Channel with Different Data_ID Tag" Case
0x321B	USE_VFIFO_TYPE	0x00	RW	Use Size Signals (12, 10, and 8) from VFIFO
0x321C	CLK_PRE_CNT	0x04	RW	Programmable Tclk_pre Time
0x3250	ISP_DP_CONF1	0x33	RW	ISP Datapath Configuration (Module Bypass/enable) Bit[7]: dpc_bc_en Black pixel correction enable in DPC Bit[6]: dpc_wc_en White pixel correction enable in DPC Bit[5]: isp_out_window_en ISP output window crop enable Bit[4]: comb_en DCG combine enable Bit[3]: lenc_en Lens correction enable Bit[2]: otp_en Defect pixel tagging enable Bit[1]: wb_gain_en WB gain enable Bit[0]: isp_en ISP enable

table A-2 sensor control registers (sheet 32 of 54)

address	register name	default value	R/W	description
0x3252	ISP_SETTING	0x20	RW	ISP Settings Bit[7]: Not used Bit[6]: real_gain_use_cg Include conversion gain when calculating real_gain Bit[5]: vsync_in_sel Select VSYNC to be used within ISP 0: From sensor_core 1: At black_row_end Bit[4]: vsync_out_sel Select VSYNC out of ISP 0: From sensor_core 1: From pre_isp Bit[3]: Not used Bit[2]: isp_pass_raw Pass 16-bit RAW value from BLC when ISP is disabled; otherwise, pass input to ISP Bit[1:0]: cfa_pattern CFA Pattern 0: Mirror 1: Flip
0x3253	PRE_CTRL0	0x00	RW	Pre_ISP Control Signals Byte 0 Bit[7]: test_mode_en Pre_ISP test mode enable Bit[6]: rolling_lines Pre_ISP rolling lines enable Bit[5]: transport_mode Pre_ISP transport mode enable Bit[4]: sq_bw Pre_ISP square black/white enable Bit[3:2]: color_bar Pre_ISP color bar style Bit[1:0]: img_sel Pre_ISP test image select 00: Bar 01: Random 10: Square 11: Chart
0x3254	PRE_CTRL1	0x11	RW	Pre_ISP Control Signals Byte 1 Bit[7:6]: Not used Bit[5:3]: hl_exp_ratio Pre_ISP HCG/LCG pixel value ratio Bit[2:0]: hvs_exp_ratio Pre_ISP HCG/VS pixel value ratio

table A-2 sensor control registers (sheet 33 of 54)

address	register name	default value	R/W	description
0x3255	PRE_CTRL2	0x01	RW	Pre_ISP Control Signals Byte 2 Bit[7]: pre_force_cg_bit_man Pre_ISP force CG bit manual override enable Bit[6]: pre_force_cg_bit Pre_ISP force CG bit value if manual override is enabled Bit[5]: Test Pre_ISP test, low byte to 0 Bit[4]: rand_img Pre_ISP random image same seed enable Bit[3:0]: rand_img_seed Pre_ISP random image seed
0x3330	LENC_RED_X0_H	0x02	RW	Red Center Horizontal Position (X0) High Byte
0x3331	LENC_RED_X0_L	0xC0	RW	Red Center Horizontal Position (X0) Low Byte
0x3332	LENC_RED_Y0_H	0x01	RW	Red Center Vertical Position (Y0) High Byte
0x3333	LENC_RED_Y0_L	0xF0	RW	Red Center Vertical Position (Y0) Low Byte
0x3334	LENC_RED_A1	0x00	RW	Red Parameter A1
0x3335	LENC_RED_A2	0x00	RW	Red Parameter A2
0x3336	LENC_RED_B1	0x00	RW	Red Parameter B1
0x3337	LENC_RED_B2	0x00	RW	Red Parameter B2
0x3338	LENC_GRN_X0_H	0x02	RW	Green Center Horizontal Position (X0) High Byte
0x3339	LENC_GRN_X0_L	0xC0	RW	Green Center Horizontal Position (X0) Low Byte
0x333A	LENC_GRN_Y0_H	0x01	RW	Green Center Vertical Position (Y0) High Byte
0x333B	LENC_GRN_Y0_L	0xF0	RW	Green Center Vertical Position (Y0) Low Byte
0x333C	LENC_GRN_A1	0x00	RW	Green Parameter A1
0x333D	LENC_GRN_A2	0x00	RW	Green Parameter A2
0x333E	LENC_GRN_B1	0x00	RW	Green Parameter B1
0x333F	LENC_GRN_B2	0x00	RW	Green Parameter B2
0x3340	LENC_BLU_X0_H	0x02	RW	Blue Center Horizontal Position (X0) High Byte
0x3341	LENC_BLU_X0_L	0xC0	RW	Blue Center Horizontal Position (X0) Low Byte
0x3342	LENC_BLU_Y0_H	0x01	RW	Blue Center Vertical Position (Y0) High Byte
0x3343	LENC_BLU_Y0_L	0xF0	RW	Blue Center Vertical Position (Y0) Low Byte

table A-2 sensor control registers (sheet 34 of 54)

address	register name	default value	R/W	description
0x3344	LENC_BLU_A1	0x00	RW	Blue Parameter A1
0x3345	LENC_BLU_A2	0x00	RW	Blue Parameter A2
0x3346	LENC_BLU_B1	0x00	RW	Blue Parameter B1
0x3347	LENC_BLU_B2	0x00	RW	Blue Parameter B2
0x3348	LENC_CTRL	0x40	RW	Bit[7]: Not used Bit[6]: lenc_bias_plus Add bias back after LENC Bit[5:4]: real_gain_sel Select real gain to use for coefficient adjustment 00: HCG 01: LCG 10: VS 11: Not used Bit[3]: coef_man_en Override LENC gain coefficient with lenc_coef_man Bit[2]: gcoef_en Enables gain coefficient adjustment Bit[1]: quad_acc_en Bit[0]: rnd_en Adds random bits
0x3349	LENC_COEF_TH	0x00	RW	Coefficient Threshold (Minimum Level of Coefficient Gain) Format: 1.7, Max: 1.0
0x334A	LENC_GAIN_THRE1_H	0x00	RW	ISP Real Gain Threshold Low (No Sub-LSB) High Byte
0x334B	LENC_GAIN_THRE1_L	0x00	RW	ISP Real Gain Threshold Low (No Sub-LSB) Low Byte
0x334C	LENC_GAIN_THRE2_H	0x00	RW	ISP Real Gain Threshold High (No Sub-LSB) High Byte
0x334D	LENC_GAIN_THRE2_L	0x00	RW	ISP Real Gain Threshold High (No Sub-LSB) Low Byte
0x334E	LENC_COEF_MAN	0x80	RW	Manual Coefficient Scaling Parameter Format: 1.7, Max: 1.0
0x3360	R_GAIN_HCG_H	0x01	RW	Gain for HCG Channel Red Component High Byte
0x3361	R_GAIN_HCG_L	0x00	RW	Gain for HCG Channel Red Component Low Byte
0x3362	GR_GAIN_HCG_H	0x01	RW	Gain for HCG Channel Greenr Component High Byte

table A-2 sensor control registers (sheet 35 of 54)

address	register name	default value	R/W	description
0x3363	GR_GAIN_HCG_L	0x00	RW	Gain for HCG Channel Greenr Component Low Byte
0x3364	GB_GAIN_HCG_H	0x01	RW	Gain for HCG Channel Greenb Component High Byte
0x3365	GB_GAIN_HCG_L	0x00	RW	Gain for HCG Channel Greenb Component Low Byte
0x3366	B_GAIN_HCG_H	0x01	RW	Gain for HCG Channel Blue Component High Byte
0x3367	B_GAIN_HCG_L	0x00	RW	Gain for HCG Channel Blue Component Low Byte
0x3368	R_GAIN_LCG_H	0x01	RW	Gain for LCG Channel Red Component High Byte
0x3369	R_GAIN_LCG_L	0x00	RW	Gain for LCG Channel Red Component Low Byte
0x336A	GR_GAIN_LCG_H	0x01	RW	Gain for LCG Channel Greenr Component High Byte
0x336B	GR_GAIN_LCG_L	0x00	RW	Gain for LCG Channel Greenr Component Low Byte
0x336C	GB_GAIN_LCG_H	0x01	RW	Gain for LCG Channel Greenb Component High Byte
0x336D	GB_GAIN_LCG_L	0x00	RW	Gain for LCG Channel Greenb Component Low Byte
0x336E	B_GAIN_LCG_H	0x01	RW	Gain for LCG Channel Blue Component High Byte
0x336F	B_GAIN_LCG_L	0x00	RW	Gain for LCG Channel Blue Component Low Byte
0x3370	R_GAIN_VS_H	0x01	RW	Gain for VS Channel Red Component High Byte
0x3371	R_GAIN_VS_L	0x00	RW	Gain for VS Channel Red Component Low Byte
0x3372	GR_GAIN_VS_H	0x01	RW	Gain for VS Channel Greenr Component High Byte
0x3373	GR_GAIN_VS_L	0x00	RW	Gain for VS Channel Greenr Component Low Byte
0x3374	GB_GAIN_VS_H	0x01	RW	Gain for VS Channel Greenb Component High Byte
0x3375	GB_GAIN_VS_L	0x00	RW	Gain for VS Channel Greenb Component Low Byte

table A-2 sensor control registers (sheet 36 of 54)

address	register name	default value	R/W	description
0x3376	B_GAIN_VS_H	0x01	RW	Gain for VS Channel Blue Component High Byte
0x3377	B_GAIN_VS_L	0x00	RW	Gain for VS Channel Blue Component Low Byte
0x3378	R_OFFSET_HCG_H	0x00	RW	Offset for HCG Channel Red Component High Byte
0x3379	R_OFFSET_HCG_M	0x00	RW	Offset for HCG Channel Red Component Middle Byte
0x337A	R_OFFSET_HCG_L	0x00	RW	Offset for HCG Channel Red Component Low Byte
0x337B	GR_OFFSET_HCG_H	0x00	RW	Offset for HCG Channel Greenr Component High Byte
0x337C	GR_OFFSET_HCG_M	0x00	RW	Offset for HCG Channel Greenr Component Middle Byte
0x337D	GR_OFFSET_HCG_L	0x00	RW	Offset for HCG Channel Greenr Component Low Byte
0x337E	GB_OFFSET_HCG_H	0x00	RW	Offset for HCG Channel Greenb Component High Byte
0x337F	GB_OFFSET_HCG_M	0x00	RW	Offset for HCG Channel Greenb Component Middle Byte
0x3380	GB_OFFSET_HCG_L	0x00	RW	Offset for HCG Channel Greenb Component Low Byte
0x3381	B_OFFSET_HCG_H	0x00	RW	Offset for HCG Channel Blue Component High Byte
0x3382	B_OFFSET_HCG_M	0x00	RW	Offset for HCG Channel Blue Component Middle Byte
0x3383	B_OFFSET_HCG_L	0x00	RW	Offset for HCG Channel Blue Component Low Byte
0x3384	R_OFFSET_LCG_H	0x00	RW	Offset for LCG Channel Red Component High Byte
0x3385	R_OFFSET_LCG_M	0x00	RW	Offset for LCG Channel Red Component Middle Byte
0x3386	R_OFFSET_LCG_L	0x00	RW	Offset for LCG Channel Red Component Low Byte
0x3387	GR_OFFSET_LCG_H	0x00	RW	Offset for LCG Channel Greenr Component High Byte
0x3388	GR_OFFSET_LCG_M	0x00	RW	Offset for LCG Channel Greenr Component Middle Byte

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address	register name	default value	R/W	description
0x3389	GR_OFFSET_LCG_L	0x00	RW	Offset for LCG Channel Greenr Component Low Byte
0x338A	GB_OFFSET_LCG_H	0x00	RW	Offset for LCG Channel Greenb Component High Byte
0x338B	GB_OFFSET_LCG_M	0x00	RW	Offset for LCG Channel Greenb Component Middle Byte
0x338C	GB_OFFSET_LCG_L	0x00	RW	Offset for LCG Channel Greenb Component Low Byte
0x338D	B_OFFSET_LCG_H	0x00	RW	Offset for LCG Channel Blue Component High Byte
0x338E	B_OFFSET_LCG_M	0x00	RW	Offset for LCG Channel Blue Component Middle byte
0x338F	B_OFFSET_LCG_L	0x00	RW	Offset for LCG Channel Blue Component Low Byte
0x3390	R_OFFSET_VS_H	0x00	RW	Offset for VS Channel Red Component High Byte
0x3391	R_OFFSET_VS_M	0x00	RW	Offset for VS Channel Red Component Middle Byte
0x3392	R_OFFSET_VS_L	0x00	RW	Offset for VS Channel Red Component Low Byte
0x3393	GR_OFFSET_VS_H	0x00	RW	Offset for VS Channel Greenr Component High Byte
0x3394	GR_OFFSET_VS_M	0x00	RW	Offset for VS Channel Greenr Component Middle Byte
0x3395	GR_OFFSET_VS_L	0x00	RW	Offset for VS Channel Greenr Component Low Byte
0x3396	GB_OFFSET_VS_H	0x00	RW	Offset for VS Channel Greenb Component High Byte
0x3397	GB_OFFSET_VS_M	0x00	RW	Offset for VS Channel Greenb Component Middle Byte
0x3398	GB_OFFSET_VS_L	0x00	RW	Offset for VS Channel Greenb Component Low Byte
0x3399	B_OFFSET_VS_H	0x00	RW	Offset for VS Channel Blue Component High Byte
0x339A	B_OFFSET_VS_M	0x00	RW	Offset for VS Channel Blue Component Middle Byte
0x339B	B_OFFSET_VS_L	0x00	RW	Offset for VS Channel Blue Component Low Byte

table A-2 sensor control registers (sheet 38 of 54)

address	register name	default value	R/W	description
0x33B0	START_ADDR_H	0x00	RW	Manual Start Address High Byte
0x33B1	START_ADDR_L	0x50	RW	Manual Start Address Low Byte
0x33B2	END_ADDR_H	0x00	RW	Manual End Address High Byte
0x33B3	END_ADDR_L	0x9F	RW	Manual End Address Low Byte
0x33B4	OTP_DPC_CTRL0	0xE2	RW	Bit[7]: otp_en_l Enable OTP-DPC for L exposure (and HDR) Bit[6]: otp_en_s Enable OTP-DPC for S exposure (and HDR) Bit[5]: otp_en_vs Enable OTP-DPC for VS exposure Bit[4]: man_inc_en Manual incremental enable signal 0: Select sensor output incremental value as input 1: Select manual set incremental value as input Bit[3]: disable_mf Mirror and flip disable signal 0: Enable mirror and flip signal 1: Disable mirror and flip input signal Bit[2]: disable_offset Manual/sensor offset select signal 0: Select sensor output offset as input offset 1: Select manual set offset as input offset Bit[1:0]: Not used
0x33B5	OTP_DPC_CTRL1	0x6F	RW	Bit[7]: Not used Bit[6:5]: recov_method Recover method Bit[4]: fixed_replace Fixed replace mode enable. Bit[3]: fixed_ptn Fixed replace pattern 0: Set every bit of cluster's recovery value with 0 1: Set every bit of cluster's recovery value with 1 Bit[2]: Not used Bit[1]: expo_en Enable sensor exposure checking Bit[0]: gain_en Enable gain checking

table A-2 sensor control registers (sheet 39 of 54)

address	register name	default value	R/W	description
0x33B6	EXPO_CONSTRAIN_L_H	0x00	RW	Exposure Constrain Value for L/S Exposure High Byte
0x33B7	EXPO_CONSTRAIN_L_L	0x00	RW	Exposure Constrain Value for L/S Exposure Low Byte
0x33B8	EXPO_CONSTRAIN_VS_H	0x00	RW	Exposure Constrain Value for VS Exposure High Byte
0x33B9	EXPO_CONSTRAIN_VS_L	0x00	RW	Exposure Constrain Value for VS Exposure Low Byte
0x33BA	GAIN_CONSTRAIN	0x02	RW	Gain Constrain Value, Real Gain Value with No Sub-LSBs
0x33BB	THRE	0x08	RW	Defects Will Only Be Corrected if Corrected Value is Larger Than Original Plus Threshold. For N Data Path, Threshold is Added to Bit[13:9], While for L and VS, Threshold is Added to Bit[9:5]. All 1s Will Turn Off Threshold.
0x33BC	MAN_X_EVEN_INC	0x01	RW	Manual Set Coordinate Incremental Value for Even Points in X Direction
0x33BD	MAN_Y_EVEN_INC	0x01	RW	Manual Set Coordinate Incremental Value for Even Points in Y Direction
0x33BE	MAN_X_ODD_INC	0x01	RW	Manual Set Coordinate Incremental Value for Odd Points in X Direction
0x33BF	MAN_Y_ODD_INC	0x01	RW	Manual Set Coordinate Incremental Value for Odd Points in Y Direction
0x33C0	MAN_X_OFFSET_H	0x00	RW	Manual Set Coordinate Offset Value for X Direction High Byte
0x33C1	MAN_X_OFFSET_L	0x00	RW	Manual Set Coordinate Offset Value for X Direction Low Byte
0x33C2	MAN_Y_OFFSET_H	0x00	RW	Manual Set Coordinate Offset Value for Y Direction High Byte
0x33C3	MAN_Y_OFFSET_L	0x00	RW	Manual Set Coordinate Offset Value for Y Direction Low Byte
0x33C4	OTP_X_OFFSET_H	–	R	OTP-DPC Output x_offset High Byte
0x33C5	OTP_X_OFFSET_L	–	R	OTP-DPC Output x_offset Low Byte
0x33C6	OTP_Y_OFFSET_H	–	R	OTP-DPC Output y_offset High Byte
0x33C7	OTP_Y_OFFSET_L	–	R	OTP-DPC Output y_offset Low Byte
0x33C8	OTP_X_EVEN_INC	–	R	OTP-DPC Output Coordinate Incremental Value for Even Points in X Direction

table A-2 sensor control registers (sheet 40 of 54)

address	register name	default value	R/W	description
0x33C9	OTP_X_ODD_INC	–	R	OTP-DPC Output Coordinate Incremental Value for Even Points in Y Direction
0x33CA	OTP_Y_EVEN_INC	–	R	OTP-DPC Output Coordinate Incremental Value for Odd Points in X Direction
0x33CB	OTP_Y_ODD_INC	–	R	OTP-DPC Output Coordinate Incremental Value for Odd Points in Y Direction
0x33E0	CTRL_DPC_00_VS	0x14	RW	DPC Control 0, VS Bit[7:6]: Not used Bit[5]: enable_tail Tail enable, enable_crosscluster must also be set Bit[4]: enable_saturate_crosscluster Saturate cross-cluster enable, enable_crosscluster must also be set Bit[3]: enable_3x3_cluster 3x3 cluster enable Bit[2]: enable_crosscluster Cross-cluster enable Bit[1]: enable_general_tail General tail enable, three horizontal connected clusters with one of pixels exceeding saturation value Bit[0]: manual_mode_en Manual mode enable
0x33E1	CTRL_DPC_01_VS	0x0F	RW	DPC Control 1, VS Bit[7:4]: Saturate Saturate pixel saturation threshold Bit[3]: enable_diffchannel_wpconn Different channel white pixel correction enable Bit[2]: enable_diffchannel_bpconn Different channel black pixel correction enable Bit[1]: enable_samechannel_wpconn Same channel white pixel correction enable Bit[0]: enable_samechannel_bpconn Same channel black pixel correction enable
0x33E2	CTRL_DPC_02_VS	0x04	RW	White Threshold List0, VS
0x33E3	CTRL_DPC_03_VS	0x02	RW	White Threshold List1, VS
0x33E4	CTRL_DPC_04_VS	0x01	RW	White Threshold List2, VS
0x33E5	CTRL_DPC_05_VS	0x01	RW	White Threshold List3, VS

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address	register name	default value	R/W	description
0x33E6	CTRL_DPC_06_VS	0x00	RW	Adaptive Pattern Thresholds, VS
0x33E7	CTRL_DPC_07_VS	0x04	RW	Adaptive Pattern Step, VS
0x33E8	CTRL_DPC_08_VS	0x0C	RW	More Connection Case Thresholds, VS
0x33E9	CTRL_DPC_09_VS	0x00	RW	DPC Level List0, VS DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality worsens.
0x33EA	CTRL_DPC_10_VS	0x01	RW	DPC Level List1, VS
0x33EB	CTRL_DPC_11_VS	0x02	RW	DPC Level List2, VS
0x33EC	CTRL_DPC_12_VS	0x03	RW	DPC Level List3, VS
0x33ED	CTRL_DPC_13_VS	0x03	RW	Gain List0, VS
0x33EE	CTRL_DPC_14_VS	0x0F	RW	Gain List1, VS
0x33EF	CTRL_DPC_15_VS	0x3F	RW	Gain List2, VS
0x33F0	CTRL_DPC_16_VS	0x08	RW	Matching Thresholds, VS If a similar pattern in neighbor of central defect pixel is found, this value will be used to determine similarity between pixels. If difference between two pixels is larger than this threshold, two are not considered similar. larger threshold will maintain more image detail.
0x33F1	CTRL_DPC_17_VS	0x04	RW	Status Thresholds, VS A pixel is marked as defective if original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x33F2	CTRL_DPC_18_VS	0x04	RW	Threshold Ratio, VS Ratio of white threshold and black threshold
0x33F3	CTRL_DPC_19_VS	0x00	RW	Clip Interpolate G Enable, VS Controls whether or not to remove defective pixels in B or R channel when G channel is saturated
0x33F4	CTRL_DPC_20_VS	0x03	RW	Edge Option, VS Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate adjacent same channel data for padding 11: Duplicate upper same channel data for padding

table A-2 sensor control registers (sheet 42 of 54)

address	register name	default value	R/W	description
0x33F5	CTRL_DPC_00_L	0x14	RW	DPC Control 0, HCG Bit[7:6]: Not used Bit[5]: enable_tail Tail enable, enable_crosscluster must also be set Bit[4]: enable_saturate_crosscluster Saturate cross-cluster enable, enable_crosscluster must also be set Bit[3]: enable_3x3_cluster 3x3 cluster enable Bit[2]: enable_crosscluster Cross-cluster enable Bit[1]: enable_general_tail General tail enable, three horizontal connected clusters with one of pixels exceeding saturation value Bit[0]: manual_mode_en Manual mode enable
0x33F6	CTRL_DPC_01_L	0x0F	RW	DPC Control 1, HCG Bit[7:4]: Saturate pixel saturation threshold Bit[3]: enable_diffchannel_wpconn Different channel white pixel correction enable Bit[2]: enable_diffchannel_bpconn Different channel black pixel correction enable Bit[1]: enable_samechannel_wpconn Same channel white pixel correction enable Bit[0]: enable_samechannel_bpconn Same channel black pixel correction enable
0x33F7	CTRL_DPC_02_L	0x04	RW	White Threshold List0, HCG
0x33F8	CTRL_DPC_03_L	0x02	RW	White Threshold List1, HCG
0x33F9	CTRL_DPC_04_L	0x01	RW	White Threshold List2, HCG
0x33FA	CTRL_DPC_05_L	0x01	RW	White Threshold List3, HCG
0x33FB	CTRL_DPC_06_L	0x00	RW	Adaptive Pattern Thresholds, HCG
0x33FC	CTRL_DPC_07_L	0x04	RW	Adaptive Pattern Step, HCG
0x33FD	CTRL_DPC_08_L	0x0C	RW	More Connection Case Thresholds, HCG

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address	register name	default value	R/W	description
0x33FE	CTRL_DPC_09_L	0x00	RW	DPC Level List0, HCG DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality worsens.
0x33FF	CTRL_DPC_10_L	0x01	RW	DPC Level List1, HCG
0x3400	CTRL_DPC_11_L	0x02	RW	DPC Level List2, HCG
0x3401	CTRL_DPC_12_L	0x03	RW	DPC Level List3, HCG
0x3402	CTRL_DPC_13_L	0x03	RW	Gain List0, HCG
0x3403	CTRL_DPC_14_L	0x0F	RW	Gain List1, HCG
0x3404	CTRL_DPC_15_L	0x3F	RW	Gain List2, HCG
0x3405	CTRL_DPC_16_L	0x08	RW	Matching Thresholds, HCG If a similar pattern in neighbor of central defect pixel is found, this value will be used to determine similarity between pixels. If difference between two pixels is larger than this threshold, two are not considered similar. larger threshold will maintain more image detail.
0x3406	CTRL_DPC_17_L	0x04	RW	Status Thresholds, HCG A pixel is marked as defective if original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x3407	CTRL_DPC_18_L	0x04	RW	Threshold Ratio, HCG Ratio of white threshold and black threshold
0x3408	CTRL_DPC_19_L	0x00	RW	Clip Interpolate G Enable, HCG Controls whether or not to remove defective pixels in B or R channel when G channel is saturated
0x3409	CTRL_DPC_20_L	0x03	RW	Edge Option, HCG Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate adjacent same channel data for padding 11: Duplicate upper same channel data for padding

table A-2 sensor control registers (sheet 44 of 54)

address	register name	default value	R/W	description
0x340A	CTRL_DPC_00_S	0x14	RW	DPC Control 0, LCG Bit[7:6]: Not used Bit[5]: enable_tail Tail enable, enable_crosscluster must also be set Bit[4]: enable_saturate_crosscluster Saturate cross-cluster enable, enable_crosscluster must also be set Bit[3]: enable_3x3_cluster 3x3 cluster enable Bit[2]: enable_crosscluster Cross-cluster enable Bit[1]: enable_general_tail General tail enable, three horizontal connected clusters with one of pixels exceeding saturation value Bit[0]: manual_mode_en Manual mode enable
0x340B	CTRL_DPC_01_S	0x0F	RW	DPC Control 1, LCG Bit[7:4]: Saturate Saturate pixel saturation threshold Bit[3]: enable_diffchannel_wpconn Different channel white pixel correction enable Bit[2]: enable_diffchannel_bpconn Different channel black pixel correction enable Bit[1]: enable_samechannel_wpconn Same channel white pixel correction enable Bit[0]: enable_samechannel_bpconn Same channel black pixel correction enable
0x340C	CTRL_DPC_02_S	0x04	RW	White Threshold List0, LCG
0x340D	CTRL_DPC_03_S	0x02	RW	White Threshold List1, LCG
0x340E	CTRL_DPC_04_S	0x01	RW	White Threshold List2, LCG
0x340F	CTRL_DPC_05_S	0x01	RW	White Threshold List3, LCG
0x3410	CTRL_DPC_06_S	0x00	RW	Adaptive Pattern Thresholds, LCG
0x3411	CTRL_DPC_07_S	0x04	RW	Adaptive Pattern Step, LCG
0x3412	CTRL_DPC_08_S	0x0C	RW	More Connection Case Thresholds, LCG

table A-2 sensor control registers (sheet 45 of 54)

address	register name	default value	R/W	description
0x3413	CTRL_DPC_09_S	0x00	RW	DPC Level List0, LCG DPC level is used to remove different types of clusters. Higher levels mean more defective clusters removed, but image quality worsens
0x3414	CTRL_DPC_10_S	0x01	RW	DPC Level List1, LCG
0x3415	CTRL_DPC_11_S	0x02	RW	DPC Level List2, LCG
0x3416	CTRL_DPC_12_S	0x03	RW	DPC Level List3, LCG
0x3417	CTRL_DPC_13_S	0x03	RW	Gain List0, LCG
0x3418	CTRL_DPC_14_S	0x0F	RW	Gain List1, LCG
0x3419	CTRL_DPC_15_S	0x3F	RW	Gain List2, LCG
0x341A	CTRL_DPC_16_S	0x08	RW	Matching Thresholds, LCG If a similar pattern in neighbor of central defect pixel is found, this value will be used to determine similarity between pixels. If difference between two pixels is larger than this threshold, two are not considered similar. larger threshold will maintain more image detail.
0x341B	CTRL_DPC_17_S	0x04	RW	Status Thresholds, LCG A pixel is marked as defective if original and recovered value is larger than this threshold. More defective pixels will be removed with a larger threshold while removing image details.
0x341C	CTRL_DPC_18_S	0x04	RW	Threshold Ratio, LCG Ratio of white threshold and black threshold
0x341D	CTRL_DPC_19_S	0x00	RW	Clip Interpolate G Enable, LCG Controls whether or not to remove defective pixels in B or R channel when G channel is saturated
0x341E	CTRL_DPC_20_S	0x03	RW	Edge Option, LCG Image boundary process option 00: Pad zero to remove white pixels 01: Pad max value to remove black pixels 10: Duplicate adjacent same channel data for padding 11: Duplicate upper same channel data for padding
0x341F	CTRL_DPC_21_VS	–	R	Black Threshold, VS
0x3420	CTRL_DPC_22_VS	–	R	White Threshold, VS
0x3421	CTRL_DPC_23_VS	–	R	Threshold 1, VS
0x3422	CTRL_DPC_24_VS	–	R	Threshold 2, VS

table A-2 sensor control registers (sheet 46 of 54)

address	register name	default value	R/W	description
0x3423	CTRL_DPC_25_VS	–	R	Threshold 3, VS
0x3424	CTRL_DPC_26_VS	–	R	Threshold 4, VS
0x3425	CTRL_DPC_27_VS	–	R	Level, VS
0x3426	CTRL_DPC_21_L	–	R	Black Threshold, HCG
0x3427	CTRL_DPC_22_L	–	R	White Threshold, HCG
0x3428	CTRL_DPC_23_L	–	R	Threshold 1, HCG
0x3429	CTRL_DPC_24_L	–	R	Threshold 1, HCG
0x342A	CTRL_DPC_25_L	–	R	Threshold 1, HCG
0x342B	CTRL_DPC_26_L	–	R	Threshold 1, HCG
0x342C	CTRL_DPC_27_L	–	R	Level, HCG
0x342D	CTRL_DPC_21_S	–	R	Black Threshold, LCG
0x342E	CTRL_DPC_22_S	–	R	White Threshold, LCG
0x342F	CTRL_DPC_23_S	–	R	Threshold 1, LCG
0x3430	CTRL_DPC_24_S	–	R	Threshold 1, LCG
0x3431	CTRL_DPC_25_S	–	R	Threshold 1, LCG
0x3432	CTRL_DPC_26_S	–	R	Threshold 1, LCG
0x3433	CTRL_DPC_27_S	–	R	Level, LCG
0x3434	DPC_STATUS	0x00	RW	DPC CRC Status Bit[7:4]: Not used Bit[3]: dpc_crc_err_wdp Allow DPC CRC error to toggle watch dog pulse Bit[2]: dpc_crc_err_vs CRC error on VS RAM occurred Bit[1]: dpc_crc_err_s CRC error on S RAM occurred Bit[0]: dpc_crc_err_l CRC error on L RAM occurred
0x3440	R_CTRL00	0x00	RW	Manual X Start Coordinate High Byte
0x3441	R_CTRL01	0x00	RW	Manual X Start Coordinate Low Byte
0x3442	R_CTRL02	0x00	RW	Manual Y Start Coordinate High Byte
0x3443	R_CTRL03	0x00	RW	Manual Y Start Coordinate Low Byte
0x3444	R_CTRL04	0x05	RW	Manual Window Width High Byte
0x3445	R_CTRL05	0x80	RW	Manual Window Width Low Byte

table A-2 sensor control registers (sheet 47 of 54)

address	register name	default value	R/W	description
0x3446	R_CTRL06	0x03	RW	Manual Window Height High Byte
0x3447	R_CTRL07	0xE0	RW	Manual Window Height Low Byte
0x3448	R_CTRL08	0x00	RW	Window Control Bit[7:5]: Not used Bit[4]: man_filter_href Window HREF signal Bit[3]: man_href_en Manual HREF control enable When enabled, use man_filter_href to decide whether to window HREF signal. When disabled, HREF will be filtered only if read_mode.always_active_dp is not set Bit[2]: flip_offset_en Flip offset enable for auto-window mode Bit[1]: mirror_offset_en Mirror offset enable for auto-window mode Bit[0]: man_win_ctrl Enable manual window control
0x3449	R_CTRL09	–	R	Read Out Pixel Count High Byte
0x344A	R_CTRL0A	–	R	Read Out Pixel Count Low Byte
0x344B	R_CTRL0B	–	R	Read Out Line Count High Byte
0x344C	R_CTRL0C	–	R	Read Out Line Count Low Byte
0x3460	GROUP_LENGTH0	0x40	RW	Number of Registers for Group 0, Total Sum of 4 Groups is Limited to 256
0x3461	GROUP_LENGTH1	0x40	RW	Number of Registers for Group 1
0x3462	GROUP_LENGTH2	0x40	RW	Number of Registers for Group 2
0x3463	GROUP_LENGTH3	0x40	RW	Number of Registers for Group 3

table A-2 sensor control registers (sheet 48 of 54)

address	register name	default value	R/W	description
0x3464	GROUP_CTRL	0x03	RW	Group Control Register, Hold Control is Bit 15 of Address Bit[7]: Not used Bit[6]: launch_now Launch immediately, when single_start is set Bit[5]: launch_pre_sof Launch before sensor core SOF, if single_start is set Bit[4]: launch_post_sof Launch after sensor core SOF, if single_start is set Bit[3:2]: first_grp_sel Main group select for hold and launch operation. Also used as first group in auto mode 00: Group select 0 01: Group select 1 10: Group select 2 11: Group select 3 Bit[1:0]: second_grp_sel Used as second group in auto mode
0x3465	FIRST_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by First Group Select
0x3466	SECOND_GRP_FRAMES	0x01	RW	Frames for Staying in Group Selected by Second Group Select
0x3467	OPERATION_CTRL	0x02	RW	Bit[7:2]: Not used Bit[1]: auto_mode Switches automatically between first and second groups using frame counts Bit[0]: single_start Launch only once, reset by logic after done, overridden by auto_mode
0x3468	EMB_START_ADDR0_H	0x30	RW	First Embedded Data Range High Byte
0x3469	EMB_START_ADDR0_L	0x00	RW	First Embedded Data Range Low Byte
0x346A	EMB_END_ADDR0_H	0x35	RW	Last Embedded Data Range High Byte
0x346B	EMB_END_ADDR0_L	0x00	RW	Last Embedded Data Range Low Byte
0x346C	ACTIVE_GROUP_NR	–	R	Indicates Which Group is Active
0x346D	FRAME_CNT_ACTIVE	–	R	Number of Frames with Current Group, Only Valid in Auto Mode

table A-2 sensor control registers (sheet 49 of 54)

address	register name	default value	R/W	description
0x3480	MIPI_CTRL0	0x00	RW	Bit[7:5]: pgm_vcm Adjust common mode voltage of HS TX Bit[4:3]: pgm_lptx Adjust driving strength of LP TX Bit[2:1]: Not used Bit[0]: bp_c_hs_en_lat Bypass ck_hs_en without mipi_pclk's latching
0x3481	MIPI_CTRL1	0x00	RW	Bit[7:5]: skew_clk Clock lane skew adjustment Bit[4]: dis_clk_lane Disable clock lane Bit[3:0]: dis_d_lane Disable data lanes
0x3482	MIPI_D_SKEW01	0x00	RW	Bit[7]: Not used Bit[6:4]: skew_d1 Data lane 1 skew adjustment Bit[3]: Not used Bit[2:0]: skew_d0 Data lane 0 skew adjustment
0x3483	MIPI_D_SKEW23	0x00	RW	Bit[7]: Not used Bit[6:4]: skew_d3 Data lane 3 skew adjustment Bit[3]: Not used Bit[2:0]: skew_d2 Data lane 2 skew adjustment
0x3484	MIPI_CTRL2	0xC0	RW	Bit[7]: mipi_lpck_retim_stb Bypass clock lane LP clock re-timing in standby Bit[6]: mipi_lpda_retim_stb Bypass data lanes LP clock retiming in standby Bit[5]: mipi_lpck_retim Bypass clock lane LP clock retiming in streaming Bit[4]: mipi_lpda_retim Bypass data lanes LP clock retiming in streaming Bit[3:0]: slew_rate MIPI slew rate

table A-2 sensor control registers (sheet 50 of 54)

address	register name	default value	R/W	description
0x3485	MIPI_CTRL3	0x80	RW	Bit[7]: mipi_man Manual MIPI lane control settings (mipi_ctrl1 bit 4 to 0) Bit[6]: mipi_data_valid_sel Reserved, keep at 0 Bit[5:4]: Ictl IVREF input bias current control Bit[3:0]: Not used
0x3486	MIPI_CONF	0x20	RW	Bit[7:6]: Not used Bit[5]: mipi_pad_stb_state Standby pad state 0: High-z 1: Pull-down Bit[4:0]: Not used
0x3487	MIPI_PADS_DIR	0x00	RW	(0: Output,1: Input, for Testing, Value to MIPI IP is Forced to 1 During Scan TM Automatically) Bit[7:5]: Not used Bit[4]: Clock lane Bit[3:0]: Data lanes
0x3488	DVP_PWR	0x00	RW	Pad Power Control Bit[7]: Not used Bit[6]: bypass_dvp_sync_fifo Bypass DVP sync fifo Bit[5]: pwdn_out Drive-value during power-down for D-pads, HREF, VSYNC, and PCLK Bit[4]: pwdn_oe Drive-enable during power-down for D-pads, HREF, VSYNC, and PCLK Bit[3:2]: pclk_pwr Drive-strength for PCLK when active Bit[1:0]: d_pwr Drive-strength for data-pins, HREF, and VSYNC pins when active
0x3489	GPIO_OE	0x00	RW	GPIO Output Enable Bit[7:2]: Not used Bit[1]: gpio1_oe GPIO1 output enable Bit[0]: gpio0_oe GPIO0 output enable

table A-2 sensor control registers (sheet 51 of 54)

address	register name	default value	R/W	description
0x348A	GPIO_OUT	0x00	RW	GPIO Output Value Bit[7:2]: Not used Bit[1]: gpio1_out GPIO1 output value Bit[0]: gpio0_out GPIO0 output value
0x348B	GPIO_CTRL	0x04	RW	Bit[7:5]: gpio_sel0 000: From gpio_out[0] 001: Row trigger 010: Temperature sensor 011: Sequencer GPIO0 100: PLL1 lock 101: PLL2 lock 110: Watchdog pulse Bit[4:3]: gpio_sel1 00: Not used 01: VSYNC 10: From gpio_out[1] 11: Sequencer GPIO1 Bit[2]: Ien GPIO input enable, must be 1 for gpio_in to be valid Bit[1:0]: Pwr Driving strength for GPIO pads
0x348C	TRIGGER_ADDR_SL_H	0x00	RW	GPIO Row Trigger Address for samp_l High Byte
0x348D	TRIGGER_ADDR_SL_L	0x01	RW	GPIO Row Trigger Address for samp_l Low Byte
0x348E	GPIO_IN	–	R	GPIO Input Value
0x348F	WDP_WIDTH	0x01	RW	Watchdog Pulse Width, Number of SCLK Cycles
0x3490	IOCTRL_10	0x15	RW	Bit[7:5]: Not used Bit[4:0]: mipi_rst_time_h[12:8] Start time for MIPI reset timer in PCLK cycles
0x3491	IOCTRL_11	0xF9	RW	Bit[7:0]: mipi_rst_time_l[7:0] Start time for MIPI reset timer in PCLK cycles
0x34A0	OTP_PGM_CTRL	0x00	RW	OTP Programming Trigger Bit[7:1]: Not used Bit[0]: otp_pgm Write 1 to program OTP, auto reset

table A-2 sensor control registers (sheet 52 of 54)

address	register name	default value	R/W	description
0x34A1	OTP_LOAD_CTRL	0x00	RW	OTP Read Trigger Bit[7:1]: Not used Bit[0]: otp_rd Write 1 to read OTP, auto reset
0x34A2	OTP_PGM_PULSE	0x80	RW	Width of Program Strobe Pulse, by 8*SCLK
0x34A3	OTP_LOAD_PULSE	0x08	RW	Width of Load Strobe Pulse, by SCLK
0x34A4	OTP_MODE_CTRL	0x00	RW	Working Mode Control Bit[7]: program_dis 0: Not used 1: Disable programing Bit[6]: mode_select 0: Auto mode 1: Manual mode Bit[5:1]: Not used Bit[0]: bank_sram_switch Switch between using bank and SRAM 0: SRAM 1: Bank
0x34A5	OTP_CTRL	0x06	RW	Bit[7:6]: Not used Bit[5]: OTP_bist_select 0: Compare with SRAM 1: Compare with 0 Bit[4]: OTP_bist_enable OTP BIST enable Bit[3]: Not used Bit[2]: OTP_pwup_load_data_enable Read OTP data on power-up Bit[1]: OTP_pwup_load_setting_en Send OTP register changes to sensor registers on power-up Bit[0]: OTP_sw_load_setting_en Send OTP register changes to sensor registers when loading OTP
0x34A7	OTP_PS2CS	0x03	RW	PS to CSB Time Control, by SCLK
0x34A8	OTP_STT_PT_H	0x00	RW	Start Address for Manual Mode High Byte
0x34A9	OTP_STT_PT_L	0x00	RW	Start Address for Manual Mode Low Byte
0x34AA	OTP_END_PT_H	0x01	RW	End Address for Manual Mode High Byte
0x34AB	OTP_END_PT_L	0xFF	RW	End Address for Manual Mode Low Byte
0x34AC	OTP_SETTING_ADR_STT_PT_H	0x00	RW	Start Address for Load Setting High Byte

table A-2 sensor control registers (sheet 53 of 54)

address	register name	default value	R/W	description
0x34AD	OTP_SETTING_ADR_ STT_PT_L	0x10	RW	Start Address for Load Setting Low Byte
0x34AE	OTP_BASE_ADR_H	0x00	RW	OTP Base Address High Byte
0x34AF	OTP_BASE_ADR_L	0x00	RW	OTP Base Address Low Byte
0x34B0	OTP_BIST_ERR_ADR_H	–	R	OTP BIST Error Address High Byte
0x34B1	OTP_BIST_ERR_ADR_L	–	R	OTP BIST Error Address Low Byte
0x34B2	OTP_STATUS	–	R	OTP Status Bit[7]: otp_pgm_o Programming ongoing Bit[6]: otp_load_o Load ongoing Bit[5]: otp_bist_err OTP BIST error Bit[4]: otp_bist_done OTP BIST done Bit[3:0]: Not used
0x34B3	OTP_CRC0	0x00	RW	OTP Content CRC Byte 0
0x34B4	OTP_CRC1	0x00	RW	OTP Content CRC Byte 1
0x34B5	OTP_CRC2	0x00	RW	OTP Content CRC Byte 2
0x34B6	OTP_CRC3	0x00	RW	OTP Content CRC Byte 3
0x7A00~ 0x7BFF	OTP_SRAM	–	–	OTP SRAM, 512x8
0x7FF0	SCCB_R0	0x00	RW	Bit[7:4]: Not used Bit[3]: sda_dly_en Enable sda_dly Bit[2:0]: sda_dly Delay SDA output by SCLK

table A-2 sensor control registers (sheet 54 of 54)

address	register name	default value	R/W	description
0x7FF1	SCCB_R1	0x12	RW	Bit[7:5]: Not used Bit[4]: en_SCCB_addr_o_inc Allow SCCB address to automatically increment Bit[3]: sda_byp_sync 0: Two clock stage synchronization for SDA input 1: No synchronization for SDA input Bit[2]: r_scl_byp_sync 0: Two clock stage synchronization for SCL input 1: No synchronization for SCL input Bit[1]: r_msk_glitch Mask glitch Bit[0]: r_msk_stop 0: Reset SCCB state machine when stop comes 1: Do nothing when stop comes
0x7FF2	SCCB_R2	0x00	RW	Bit[7:4]: r_sda_num Number of SCLK cycles SDA must be constant for value to be used internally Bit[3:0]: r_scl_num Number of SCLK cycles SCL must be constant for value to be used internally
0x7FF6	SCCB_CRC_H	–	R	SCCB CRC High Byte
0x7FF7	SCCB_CRC_L	–	R	SCCB CRC Low Byte

revision history

version 1.0 07.10.2018

- initial release

version 1.1 08.16.2018

- in ordering information, changed ordering part numbers to OV09716-B77Y-1E-Z, OV09716-B77Y-LE-Z, and OV09716-B77Y-OE-Z
- in key specifications, changed power supply to "SVDD, SVDD_pix, PVDD (analog): 3.14 ~ 3.47V, DVDD (digital): 1.14 ~ 1.3V, DOVDD (digital): 1.7 ~ 1.9V, AVDD18 (analog): 1.7 ~ 1.9V", and changed max S/N ratio to 41 dB
- in section 1.1, changed third sentence of second paragraph to "The sensor supports dual exposure staggered HDR for 120 dB." and changed last sentence of second paragraph to "In this case, the HDR combination is done externally from the 16-bit first plus 12-bit second exposure output."
- in section 1.3, removed first sentence of first paragraph, changed second sentence (previously third sentence) of first paragraph to "The SCCB ID is defined by the voltage level of GPIO1 at power up and after hardware reset (RESETB pin low).", added new third and fourth sentences to first paragraph, changed sixth sentence of last paragraph to "The recommended capacitance is 1µF.", updated figures 1-4, and added new figure 1-5
- in section 1.4, moved section 1.4.2 before figure 1-6 (previously figure 1-5), added new section 1.4.2 immediately before figure 1-6, and updated figure 1-6
- in section 1.4.1 (previously section 1.4.2), moved first paragraph to end of section, changed fifth paragraph (previously sixth paragraph) to "IO pins' states are described according to table 1-2 (column for RESETB = 0)", and changed seventh paragraph (previously eighth paragraph) to "SCCB is disabled"
- in section 1.4.2 (previously section 1.4), changed second sentence of first paragraph to "When the POR is released, the sensor finishes the hardware reset (HW_RESET) and enters software reset state (SW_RESET)...", changed third sentence of first paragraph to "To extend the HW_RESET period, keep the RESETB pin low.", removed fourth sentence of first paragraph, and changed last sentence of first paragraph to "SW_RESET can also be reached from any other state by writing the software reset register bit via SCCB."
- in section 1.4.3 (previously section 1.4.1), removed "a power-saving" from second sentence of first paragraph
- in section 1.4.4 (previously section 1.4.3), changed second sentence of first paragraph to "When the PLLs are stable after 4096 XVCLK cycles, the main clocks are switched from XVCLK to the faster PLL clocks, and the integration starts.", and changed third sentence of first paragraph to "After the integration period elapses, video data output starts."
- in section 1.4.5 (previously section 1.4.4), removed last paragraph
- in chapter 2, changed first sentence of fourth paragraph to "The OV9716 offers dual conversion gain (DCG) HDR, which means the pixels are read out at both low and high conversion gain...", removed last sentence of fourth paragraph, and changed fifth paragraph to "The OV9716 also supports staggered very short exposure (VS) to extend the dynamic range to 120 dB. In this mode, HCG and LCG combination..."
- in section 3.2, changed third sentence of first paragraph to "The crop registers in address 0x30A0~0x30A7..."

- in section 3.6, changed third paragraph to "where Tsclk is the system clock period and Fsclk is the system clock frequency."
- in section 3.7.1, changed first paragraph to "Conversion gain is controlled by register 0x30BB[6], where '1' means high conversion gain and '0' means low conversion gain."
- in section 3.8.1, changed first sentence of fifth paragraph to "Continuously updating the correction values in BLC may lead to undesired flickering, hence BLC trigger-mode is implemented.", changed second sentence of fifth paragraph to "When BLC is in trigger-mode, the correction values remain unchanged until a condition (trigger) occurs.", changed first sentence of sixth paragraph to "When triggered, the correction values in BLC are updated continuously…", removed "like in previous sensors" from fourth sentence of seventh paragraph, changed fifth sentence of seventh paragraph to "It is assumed that the VS exposure is later than the DCG exposure when triggered, ensuring that the VS exposure BLC is triggered in the same frame as the DCG exposure." and changed ninth paragraph to "If triggering is not enabled, the correction values are updated in every frame. When filtering is enabled, the correction value is still directly applied upon a hard trigger."
- in section 3.9, changed last sentence of second paragraph to "Additionally, in MIPI mode, the two PLLs can be used to optimize the MIPI frequency to minimize EMI.", and removed "in many interface design" from fifth sentence of third paragraph
- in chapter 4, updated figure 4-1
- in section 4.1, changed second sentence of first paragraph to "The analog test pattern is a color bar overlaid with pixel output to excise the whole analog readout channel", added new third sentence to first paragraph, and changed last sentence of first paragraph to "The input data of test pattern is unaffected by sensor exposure time and gain, however, the ISP processing parameters may be still dependent on the gain."
- in section 4.5, changed second bullet to "For single exposure HDR mode, data output can...(HCG_analog_gain x HCG_digital_gain)/(LCG_analog_gain x LCG_digital_gain) should not be greater than 1.6.", changed last sentence of third bullet to "Ratio between LCG and VS is determined by exposure time and gain", changed third bullet to last, and removed fourth bullet
- in table 5-1, removed "DCG" from dual exposure HDR formats 3x12b DCG, 3x10b compressed DCG, 12b RAW DCG (HCG or LCG) + 12b VS, and removed "DCG" from single exposure HDR format 2x12b DCG
- in table 5-3, removed "DCG" from dual exposure HDR formats 3x12b DCG, 3x10b compressed DCG, 12b RAW DCG (HCG or LCG) + 12b VS, removed "DCG" from single exposure HDR format 2x12b DCG, changed sixth register setting column to first column, changed fifth register setting column to second column, changed fourth register setting column to third column, changed third register setting column to fourth column, changed second register setting column to fifth column, and changed first register setting column to sixth column
- in section 5.2.1, changed title to "DCG 16b to compressed DCG 12b", and changed first paragraph to "The OV9716 has a data compression from DCG 16-bit to compressed DCG 12-bit..."
- in section 5.2.2, changed title to "linear 12b to linear 10b", and changed first paragraph to "The OV9716 has a data compression from linear 12-bit to linear 10-bit..."
- in section 5.3, changed all references to "PA" to "P_A", changed all references to "PB" to "P_B", and changed all references to "PC" to "P_C",
- in section 5.3.1, added new last sentence to first paragraph, changed first sentence of second paragraph to "For non-staggered HDR, the OV9716 outputs multiple captures over different virtual channels or one single shared virtual channel...", changed third paragraph to "For staggered HDR, the OV9716 outputs multiple captures over different virtual channels or one single shared virtual channel...", and updated figures 5-3, 5-4, 5-5, 5-6, 5-7, 5-8, 5-9, and 5-10
- in table 5-4, removed "DCG" from dual exposure HDR formats 3x12b (3x10b) DCG, 12b RAW DCG (HCG or LCG) + 12b VS, and removed "DCG" from single exposure HDR format 2x12b DCG
- in section 5.3.1.1, updated figure 5-11

- in figure 5-12, changed title to "16b DCG + 12b VS dual HDR diagram" and updated figure
- in figure 5-13, changed title to "12b compressed DCG + 12b VS dual HDR diagram" and updated figure
- in section 5.3.1.4, changed title to "3x12b (3x10b) HDR"
- in figure 5-14, changed title to "3x12b (3x10b) HDR diagram" and updated figure
- in section 5.3.1.5, updated figure 5-15
- in section 5.3.1.6, updated figure 5-16
- in section 5.3.1.7, updated figure 5-17
- in section 5.3.1.8, changed title to "2x12b single HDR (VC0/VC1)"
- in figure 5-18, changed title to "2x12b single HDR (VC0/VC1) diagram" and updated figure
- in section 5.3.2, moved figure 5-20 immediately before figure 5-19, moved figure 5-22 immediately following table 5-8, and updated figure 5-22
- in table 5-8, removed "DCG" from dual exposure HDR format 12b RAW DCG (HCG or LCG) + 12b VS and removed "DCG" from single exposure HDR format 2x12b DCG
- in section 5.3.2.1, updated figure 5-23
- in section 5.3.2.2, changed title to "12b RAW (HCG or LCG) + 12b VS dual HDR"
- in figure 5-24, changed title to "12b RAW (HCG or LCG) + 12b VS diagram" and updated figure
- in section 5.3.2.3, updated figure 5-25
- in section 5.3.2.4, changed title to "2x12b single HDR"
- in figure 5-26, changed title to "2x12b single HDR diagram"
- in section 5.4.1, updated figure 5-27
- in section 5.5.1, changed "AWB" to "WB" in first bullet
- in section 5.6, changed last sentence of first paragraph to "Embedded data can be enabled in the image by setting register..." and removed second paragraph
- in section 5.6.1, changed last sentence of second paragraph to "For example, embedded data will be added in the HCG captures for 3x12b and in the LCG captures for 12b LCG +12b VS."
- in section 5.7, added "The group hold function is controlled through registers 0x3460~0x346D." to end of first paragraph, and removed third paragraph
- in section 5.8.2, changed fifth sentence of first paragraph to "...(i.e., they hold the previous CRC value until a new SCCB write occurs after any of the CRC registers are read)."
- in section 6.1, updated figure 6-1 and added table 6-2
- in table 6-1, changed title to "SCCB interface timing specifications based on 400 kHz", removed max value for f_{SCL}, removed row for t_{DH}, and removed table footnotes a and c

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- in key specifications, changed operating temperature to -40°C to 105°C sensor ambient temperature and -40°C to 132°C junction temperature
- in section 1.4.2, updated figure 1-6
- in table 1-4, removed row for T_{PWDN} and changed min value for T_{RST} to 1 ms
- in table 8-2, changed operating temperature range to -40°C to +132°C sensor junction temperature
- in table 8-3, changed title to "...< 132°C)", changed fifth column title to "max @ 132°C", replaced all TBDs, added min and max @ 132°C values for $V_{DD-3.3}$, $V_{DD-1.2}$, and $V_{DD-1.8}$, added max @ 132°C

values for $I_{DD-3.3}$, $I_{DD-1.2}$, $I_{DD-1.8}$, $I_{DDS-PWDNB-3.3}$, $I_{DDS-PWDNB-1.2}$, and $I_{DDS-PWDNB-1.8}$, and changed table footnote a to "active current based on 30 fps settings"

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- in table 8-3, changed max @ 132°C value for $I_{DD-1.2}$ to 150 mA

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- in section 3.10, changed end of second sentence to "...is enabled by register {0x3066}.", changed end of third sentence to "...read back by registers {0x3067, 0x3068}", and added new fourth, fifth, and sixth sentences

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