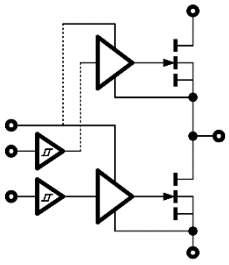
650 V GaNFast™ Power IC

QFN 6 x 8 mm



Simplified schematic

1. Features

GaNFast Power IC

- Two independent logic inputs with hysteresis
- Enable Input
- Ultra-low standby current
- Wide V_{CC} range
- Low-side turn-on dV/dt slew rate control
- 200 V/ns dV/dt immunity
- ESD, high-side UVLO, shoot-through protection
- Floating high-side with internal level shifter
- Integrated high-side bootstrap
- High-frequency operation up to 2Mhz

650 V eMode GaN FETs

- 600 mΩ high-side FET
- 300 mΩ low-side FET
- Zero reverse recovery charge

Small, low-profile SMT QFN

- 6 x 8 mm footprint, 0.85 mm profile
- Minimized package inductance
- RoHS, Pb-Free, REACH-complaint

2. Description

The NV6252 is a high-performance, easy-to-use, 650 V half-bridge GaNFast power IC, optimized for high-frequency, soft-switching topologies.

The feature-rich, monolithically-integrated GaNFast power IC with simple logic inputs, harnesses two high-performance eMode GaN FETs (600 mΩ high-side, 300 mΩ low-side) to create the fastest, smallest, most efficient powertrain in the world.

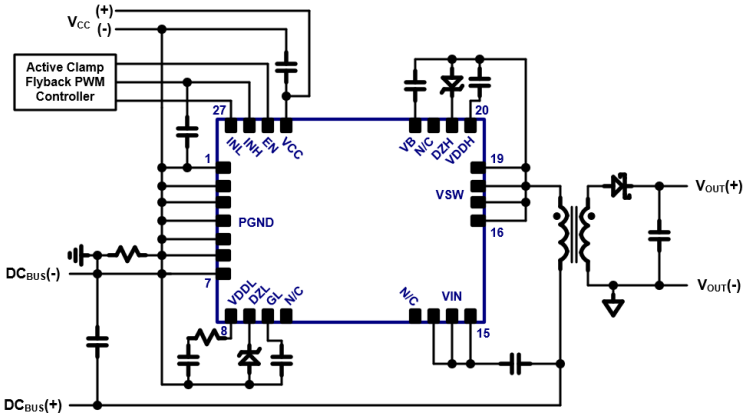
The highest dV/dt immunity, integrated protection features and industry-standard low-profile, low-inductance, 6x8 mm SMT QFN package combine to enable designers to exploit GaN technology with simple, quick, dependable solutions achieving breakthrough power density and efficiency

GaNFast power ICs extend the capabilities of traditional topologies such as flyback, half-bridge, buck/boost, resonant, etc. to MHz+ and enable the commercial introduction of breakthrough designs.

3. Topologies / Applications

- AC-DC, DC-DC, DC-AC
- Buck, boost, half bridge, full bridge
- Active Clamp Flyback, LLC resonant, Class D
- Mobile fast-chargers, adapters
- Notebook adaptors
- LED lighting, TV / monitor
- Server, telecom aux power

Typical Application Circuits



4. Table of Contents

5. Specifications

5.1. Absolute Maximum Ratings (1)

(with respect to **P_{GND}** unless noted)

SYMBOL	PARAMETER	MAX	UNITS
V_{IN}	HV input	-7 to +650	V
V_{SW}	Switch Node	-7 to +657	V
V_{CC}	Supply Voltage	30	V
V_B	High-side gate driver bootstrap rail (to V_{SW})	30	V
V_{DZL}	Low-side voltage regulator setting input	6.6	V
V_{DZH}	High-side voltage regulator setting input (to V_{SW})	6.6	V
V_{DDL}	Low-side Drive Supply Voltage	7.2	V
V_{DDH}	High-side Drive Supply Voltage (to V_{SW})	7.2	V
V_{INH}, V_{INL}	High-/Low-side driver input	V_{CC}	V
V_{EN}	Enable drive input	V_{CC}	V
V_{GL}	Low-side Gate Voltage	7.2	V
I_{OUTL}	Continuous Drain Current (@ T_C = 100ºC, Low-side FET)	5	A
I_{OUTH}	Continuous Drain Current (@ T_C = 100ºC, High-side FET)	3	A
I_{OUTL} PULSE	Pulsed Drain Current (10 µs @ T_J = 25°C, Low-side FET)	9	A
I_{OUTH} PULSE	Pulsed Drain Current (10 µs @ T_J = 125°C, High-side FET)	6	A
dV/dt	Slew Rate on Drain-to-Source	200	V/ns
T_J	Operating Junction Temperature	-55 to 150	ºC
T_{STOR}	Storage Temperature	-55 to 150	ºC

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

5.2. Recommended Operating Conditions (2)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DZL}	Low-side Drive Supply Set Zener Voltage (3)	5.8	6.2	6.6	V
V_{DZH}	High-side Drive Supply Set Zener Voltage (3)	5.8	6.2	6.6	V
R_{DD}	Gate Drive Turn-On Current Set Resistance	0	0	100	Ω
V_{INH}, V_{INL}	High-/Low-side drive/Enable input	0	5	V_{CC}	V
V_{EN}	Enable drive input	0	5	V_{CC}	V
$V_{IN,}$ V_{SW}	Drain-to-Source Voltage			480	V
V_{CC}	Supply Voltage	10		24	V
T_J	Operating Junction Temperature	-40		125	°C

(2) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.
(3) Use of zener diode other than 6.2 V is not recommended. See Table I for recommended part numbers of 6.2 V zener diodes.

5.3. ESD Ratings

SYMBOL	PARAMETER	MAX	UNITS
HBM	Human Body Model (per JS-001-2014)	1,000	V
CDM	Charged Device Model (per JS-002-2014)	500	V

5.4. Thermal Resistance

SYMBOL	PARAMETER	TYP	UNITS
$R_{\theta JC}$ (4)	Junction-to-Case	1.8	ºC/W
$R_{\theta JA}$ (4)	Junction-to-Ambient	40	ºC/W

(4) R_{θ} measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

5.5. Electrical Characteristics

Typical conditions: V_{IN} = 400 V, V_{CC} = 15 V, V_{DZL} = 6.2 V, V_{DZH} = 6.2 V, T_{AMB} = 25 ºC, I_{OUT} = 1.5 A (or specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC} Supply Characteristics						
V_{CCUV+}	V_{CC} UVLO Rising Turn-On Threshold		9.25	10	V	
V_{CCUV-}	V_{CC} UVLO Falling Turn-Off Threshold		8.75		V	
V_{CCUV_HYS}	V_{CC} UVLO Hysteresis		0.5		V	
I_{QCC_STBY}	V_{CC} Standby Current		195		µA	V_{IN} = 0 V, V_{EN} = 0 V, I_{SW} = 0 A, V_{SW} = 15 V
I_{QCC}	V_{CC} Quiescent Current		4.0		mA	V_{INH} = 0 V, V_{INL} = 0 V, V_{EN} = 6 V, V_{SW} = 15 V
I_{CC_SW}	V_{CC} Switching Current		11.5		mA	F_{SW} = 1 MHz
V_B Supply Characteristics						
VB_{UV+}	V_B UVLO Rising Turn-On Threshold (V_B – V_{SW})		10	11	V	
VB_{UV-}	V_B UVLO Falling Turn-Off Threshold (V_B – V_{SW})		9.5		V	
VB_{HYS}	V_B UVLO Hysteresis		0.5		V	
I_{QVB}	V_B Quiescent Current		4.6		mA	V_{INH} = 0 V, V_{INL} = 0 V, V_{SW} = 0 V, V_B = 15 V
Bootstrap FET Characteristics						
I_{BOOT}	Bootstrap Charging Current		1		A	V_B = 0 V, V_{SW} = 0 V
V_{BDROP}	Bootstrap Voltage Drop		0.15		V	V_{SW} = 0 V, F_{SW} = 1 MHz
Logic Inputs Characteristics						
$V_{INH,L+}$	Input Logic High Threshold (rising edge)			4	V	
$V_{INH,L-}$	Input Logic Low Threshold (falling edge)	1			V	
V_{I_HYS}	Input Logic Hysteresis		0.5		V	
t_{INHPLH}	Prop Delay (IN_H from Low to High, V_{SW} pulled to V_{IN})		40		ns	Fig.1
t_{INHPHL}	Prop Delay (IN_H from High to Low, V_{SW} tri-stated)		40		ns	Fig.2
t_{INLPLH}	Prop Delay (IN_L from Low to High, V_{SW} pulled to P_{GND})		15		ns	Fig.3
t_{INLPHL}	Prop Delay (IN_L from High to Low, V_{SW} tri-stated)		15		ns	Fig.4
Enable Input Characteristics						
V_{EN+}	IC Enable Rising Turn-on Threshold			4	V	
V_{EN-}	IC Enable Falling Turn-off Threshold	0.75			V	
V_{EN_HYS}	IC Enable Hysteresis		0.5		V	
Switching Characteristics						
F_{SW}	Switching Frequency			2	MHz	
t_{PW}	Pulse width	0.05		1000	µs	High side, no low side min

Electrical Characteristics (Cont.)

Typical conditions: V_{IN} = 400 V, V_{CC} = 15 V, V_{DZL} = 6.2 V, V_{DZH} = 6.2 V, T_{AMB} = 25 ºC, I_{OUT} = 1.5 A (or specified)

High-side GaN FET Characteristics						
$R_{DS(ON)}$	High-side FET Drain-Source Resistance		600	800	mΩ	V_{INL} = 0 V, V_{INH} = 6 V, I_D = 1.5 A
V_{SD}	Source-Drain Reverse Voltage		2.4		V	V_{INL} = 0 V, V_{INH} = 0 V, I_{SD} = 1 A
Q_{OSS}	Output Charge		8		nC	V_{DS} = 400 V, V_{INL} = 0V, V_{INH} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	V_{DS} = 400 V
C_{OSS}	Output Capacitance		8		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(er)}$ (5)	Effective Output Capacitance, Energy Related		12		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(tr)}$ (6)	Effective Output Capacitance, Time Related		19		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
Low-side GaN FET Characteristics						
$R_{DS(ON)}$	Low-side FET Drain-Source Resistance		300	400	mΩ	V_{INL} = 6 V, V_{INH} = 0 V, I_D = 3 A
V_{SD}	Source-Drain Reverse Voltage		2		V	V_{INL} = 0 V, V_{INH} = 0 V, I_{SD} = 1 A
Q_{OSS}	Output Charge		14		nC	V_{DS} = 400V, V_{INL} = 0 V, V_{INH} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	V_{DS} = 400 V
C_{OSS}	Output Capacitance		14		pF	V_{DS} = 400V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(er)}$ (5)	Effective Output Capacitance, Energy Related		20		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(tr)}$ (6)	Effective Output Capacitance, Time Related		32		pF	V_{DS} = 400 V, V_{INL} =0 V, V_{INH} = 0 V

(5) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(6) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

5.6. Switching Waveforms

(T_C = 25 ºC unless otherwise specified)

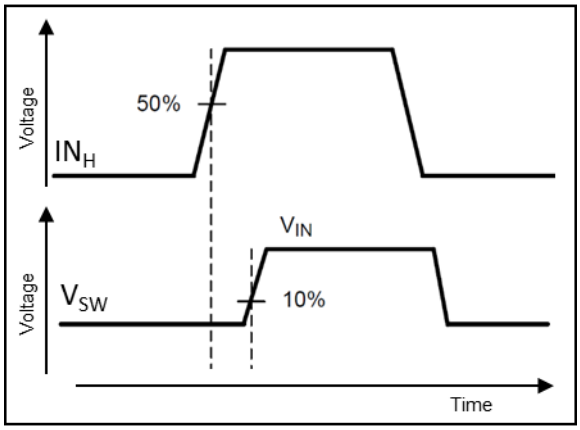


Fig.1. Propagation Delay Buck Mode t_{INHPLH}

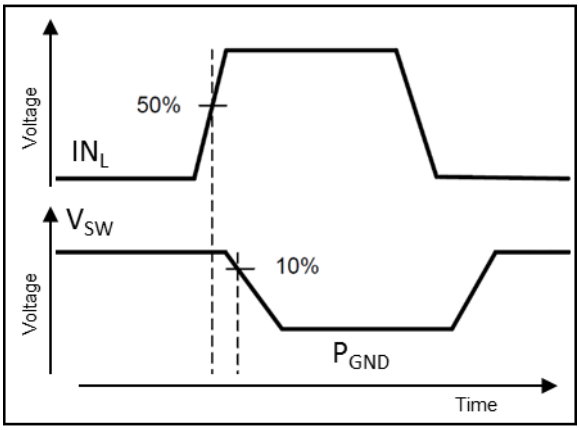


Fig.2. Propagation Delay Boost Mode t_{INHPHL}

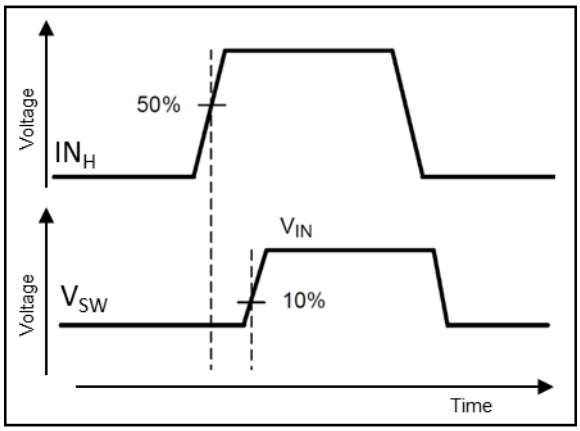


Fig.3. Propagation Delay Buck Mode t_{INLPLH}

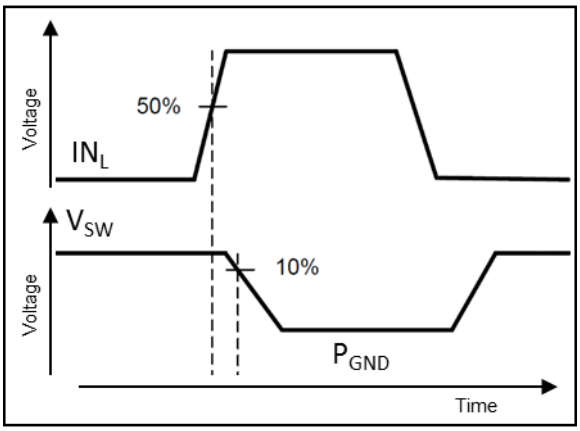


Fig.4. Propagation Delay Boost Mode t_{INLPHL}

5.7. Characteristic Graphs

(GaN FET, T_C = 25 ºC unless otherwise specified)

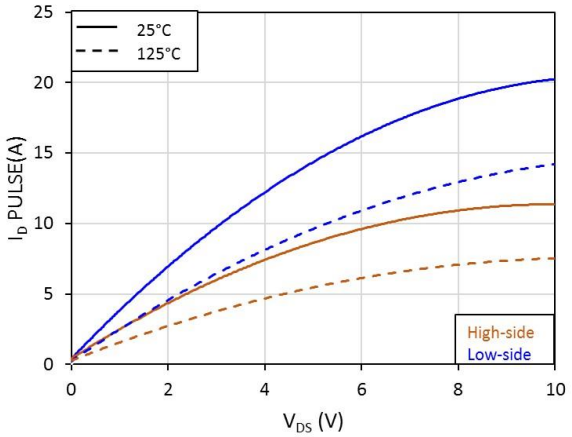


Fig.5. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS})

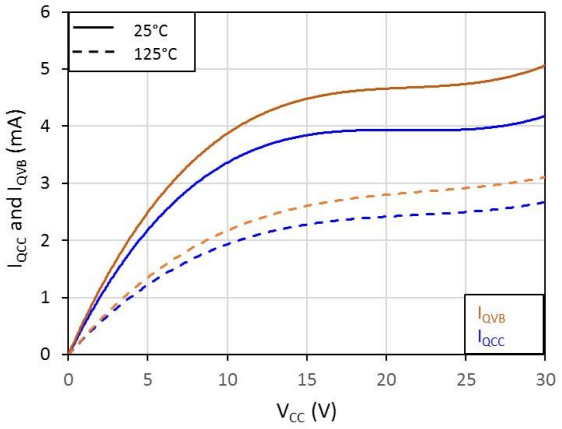


Fig.6. V_{CC} and V_B quiescent current (I_{QCC} and I_{QVB} vs. supply voltage (V_{CC})

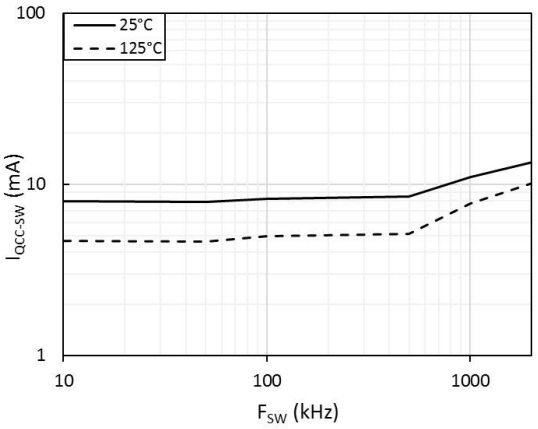


Fig.7. V_{CC} operating current (I_{CC-SW}) vs. operating frequency (F_{SW})

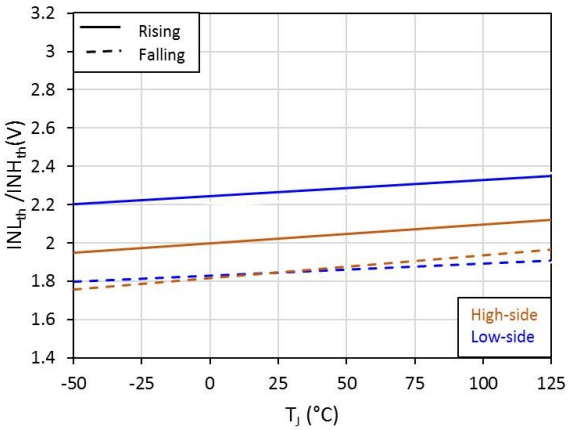


Fig.8. INL_{th} and INH_{th} vs. junction temperature (T_J)

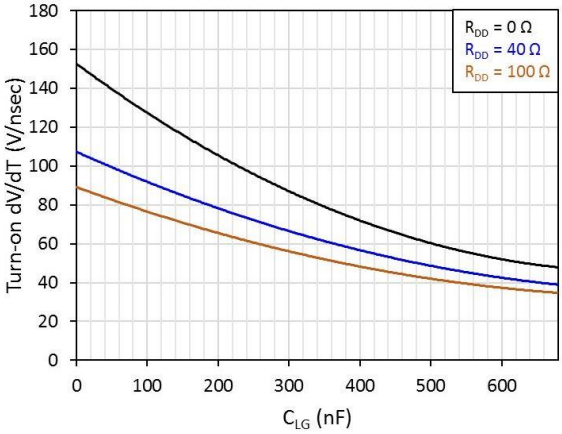


Fig.9. Slew rate (dV/dt) vs. low-side gate capacitance (C_{GL})

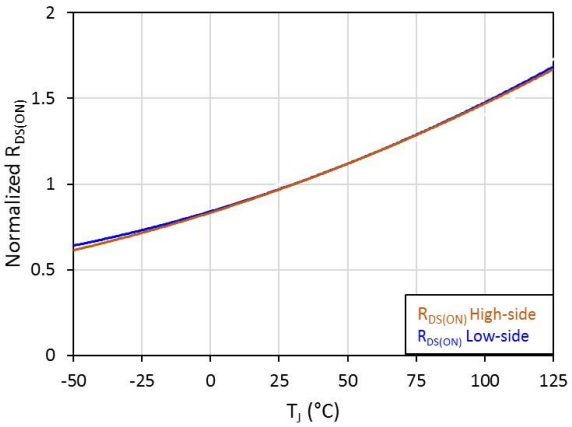


Fig.10. Normalized on-resistance ($R_{DS(ON)}$) vs. junction temperature (T_J)

Characteristic Graphs (Cont.)

(GaN FET, T_C = 25 ºC unless otherwise specified)

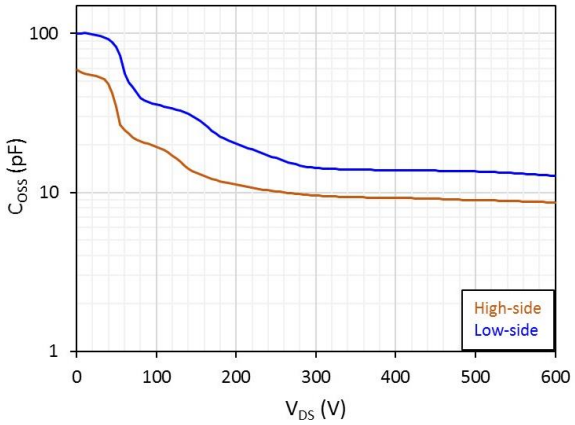


Fig.11. Output capacitance (C_{OSS}) vs. drain-to-source voltage (V_{DS})

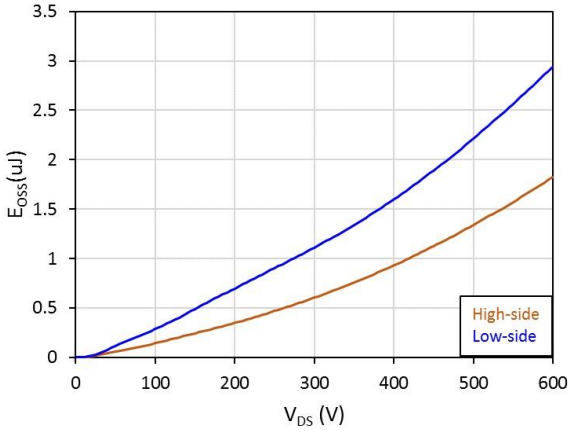


Fig.12. Energy stored in output capacitance (E_{OSS}) vs. drain-to-source voltage (V_{DS})

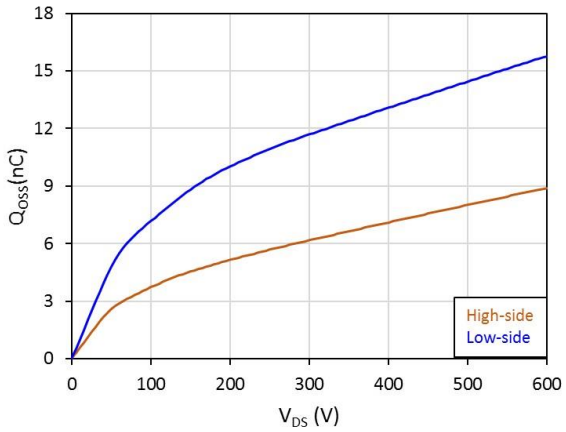


Fig.13. Charge stored in output capacitance (Q_{OSS}) vs. drain-to-source voltage (V_{DS})

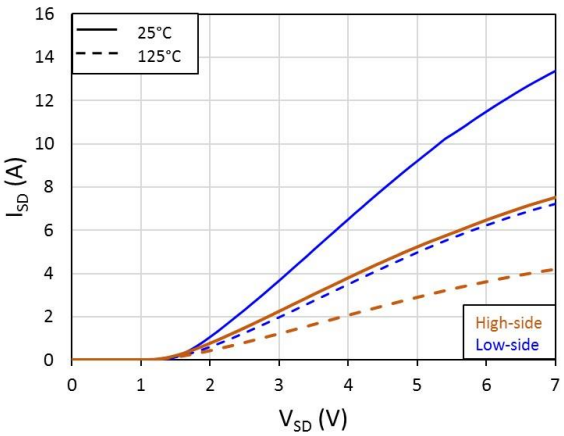


Fig.14. Source-to-drain reverse conduction voltage

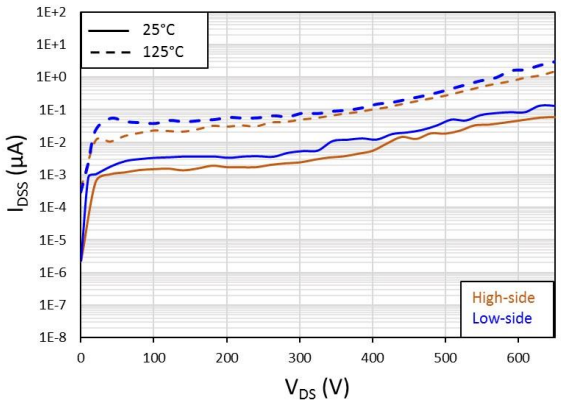
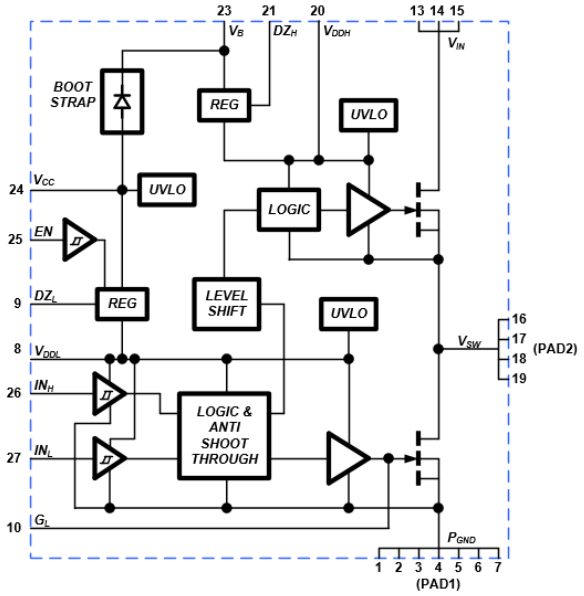
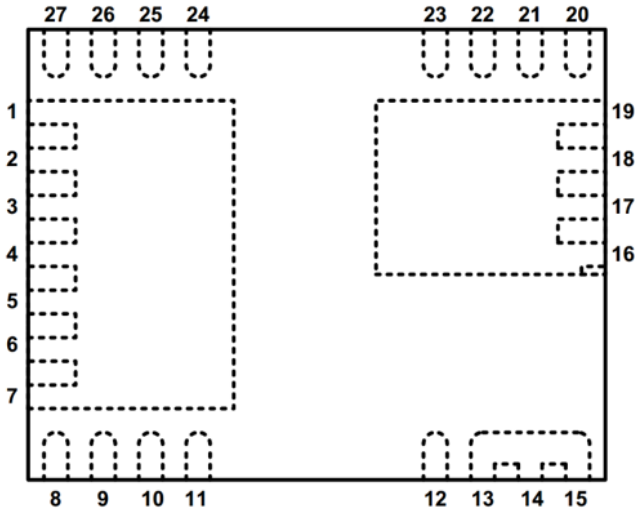


Fig.15. Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS})

6. Internal Schematic, Pin Configurations and Functions





Package Top View

Pin		I/O[1]	Description
Number	Symbol		
1 – 7 (and large pad)	P_{GND}	G	Power ground
8	V_{DDL}	P	Low-side drive supply
9	D_{ZL}	I	V_{DDL} set voltage (6.2V Zener to P_{GND})
10	G_L	O	Low-side gate
11	N/C		No connect
12	N/C		No connect
13 – 15	V_{IN}	P	HV input
16 – 19 (and small pad)	V_{SW}	O	Half-bridge switch Node
20	V_{DDH}	P	High-side drive supply
21	D_{ZH}	I	V_{DDH} set voltage (6.2V Zener to V_{SW})
22	N/C		No connect
23	V_B	P	High-side gate driver bootstrap rail
24	V_{CC}	P	IC supply voltage
25	EN	I	IC enable input (1=ON)
26	IN_H	I	High-side drive input
27	IN_L	I	Low-side drive input

(1) I = Input, O = Output, P = Power, G = GaN IC Ground

7. Functional Description

The NV6252 includes many functions designed for proper half-bridge operation during different circuit operating modes. The following functional description contains additional information regarding the IC operating modes and pin functionality.

7.1. Start Up

The NV6252 includes integrated UVLO circuits for disabling the IC when V_{CC}, V_{DDL} and V_B are below their respective UVLO+ thresholds. During UVLO Mode, the gate drive and half-bridge power FETs are disabled and V_{CC} consumes a low current. At start-up when the V_{CC} supply voltage increases (Fig.17), the voltages at the V_{DDL} pin and the DZ_L pin both increase as well. The V_{DDL} supply voltage will exceed the V_{DDUV+} threshold (4.8V typical) and then get limited by the internal regulator to the voltage level set by the Zener diode at the DZ_L pin (6.2 V, typical). The Zener diodes at the DZ_L and DZ_H pins should be a low-current type with a flat Zener voltage curve (above the knee) in the sub-100 µA current range (see Table III for recommended Zener diode part numbers). The V_{CC} voltage continues to increase until it exceeds the VCC_{UV+} threshold (9.25V typical) and the IC enters Normal Operating Mode. Initially, only the low-side half-bridge FET will turn on with the IN_L PWM input signal. The high-side supply V_B charges up through the internal bootstrap FET during the IN_L on-time. When V_B exceeds the VB_{UV+} threshold (10V typical), the high-side circuitry will be enabled and the high-side FET will turn on with the next IN_H PWM input signal.

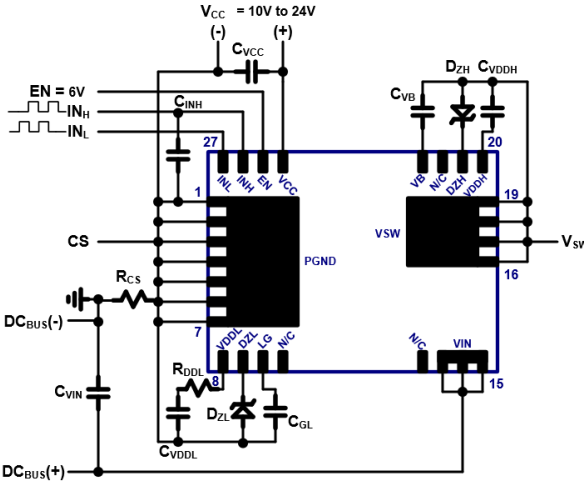


Fig.16. Quick start-up circuit

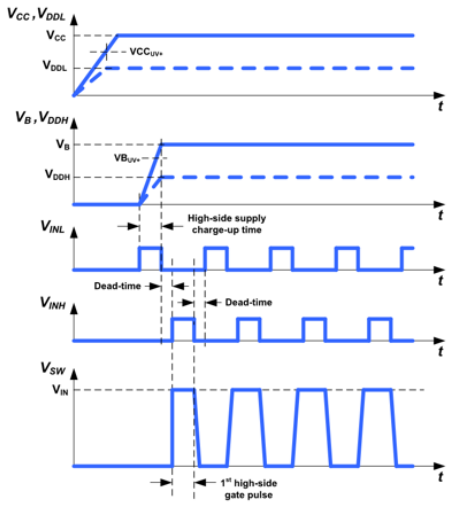


Fig.17. Start-up timing diagram

7.2. Normal Operating Mode

During normal operating mode, the EN pin is above the V_{EN+} threshold (4V maximum), V_{CC} is being regulated at a sufficient level (15 V typical) by the auxiliary power supply of the power converter, and V_B is at a sufficient level (as set by V_{CC} and the internal bootstrap circuit). The PWM input signals at the IN_L and IN_H pins turn the gates of the internal high- and low-side power FETs on and off at the desired duty-cycle, frequency and dead-time. The input logic signal at the IN_L pin turns the low-side half-bridge power FET on and off (0=OFF, 1=ON), and the input logic signal at the IN_H pin turns the high-side half-bridge power FET on and off (0=OFF, 1=ON). As the PWM inputs are turned on and off in a complementary manner each switching cycle, the V_{SW} pin (half-bridge mid-point) is then switched between P_{GND} (IN_L=1, IN_H=0) and V_{IN} (IN_L=0, IN_H=1) at the given frequency and duty-cycle (Fig.16). The NV6252 includes shoot-through protection circuitry that prevents both power FETs from turning on simultaneously. The IC also includes an internal bootstrap FET for supplying the high-side circuitry. The bootstrap FET is enabled during normal operating mode and is turned on each PWM switching cycle only when the IN_L pin is 'HIGH" and the low-side power FET is on. This will allow the V_B capacitor to be charged up each switching cycle for properly maintaining the necessary high-side supply voltage. The V_B capacitor value should be sized correctly such that the V_B voltage is maintained at a sufficient level above UVLO- during normal operation. Should the V_B-V_{SW} voltage decrease below the falling VB_{UV-} UVLO threshold (9.5V typical) at any time, then

the high-side power FET will turn off and become disabled until V_B-V_{SW} increases again above the VB_{UV+} threshold (10V typical).

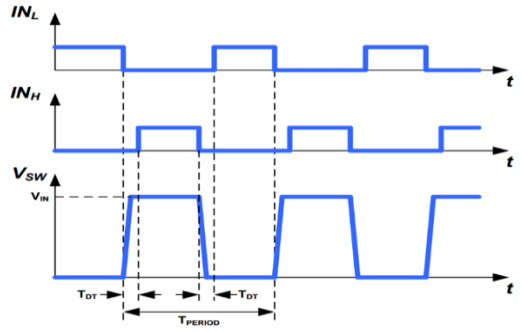


Fig.18. Normal operating mode timing diagram

7.3. Standby Mode

The NV6252 includes an Enable input (EN pin) for disabling the IC and reducing the V_{CC} current consumption. To disable the IC and enter low-current Standby Mode, the EN pin is decreased below the V_{EN-} threshold (0.75V min). This will disable both half-bridge FETs and reduce V_{CC} current consumption to a low level 130 uA typical). DZ_L will remain held at its Zener voltage and V_{DDL} will slowly discharge to P_{GND}. When the EN pin voltage is increased again above the V_{EN+} threshold (4V max), the IC will become enabled and V_{DDL} will charge up again above the V_{DDUV+} threshold and the IC will start up (Fig.19). An external MOSFET can be used to pull the EN pin down to the P_{GND} potential. If an enable signal is available that is greater than the V_{DDL} voltage, then a diode can be used to pull down the EN pin. If an active standby signal is available from the controller then this signal can be used to pull down the EN pin directly with no additional external components required.

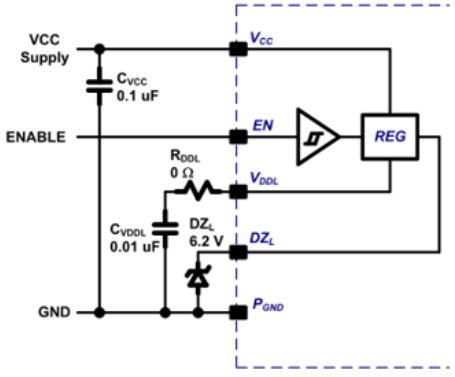


Fig.19. Standby mode V_{CC} cut-off circuit

7.4. Programmable Turn-on dV/dt Control

During first start-up pulses or during hard-switching conditions, it is desirable to limit the slew rate (dV/dt) of the drain of the low-side power FET during turn-on. This is necessary to reduce EMI or to reduce circuit switching noise. The turn-on slew rate of the low-side power FET is already reduced by default internally to a low level. To reduce the turn-on dv/dt rate of the internal low-side power FET further, an external capacitor (C_{GL}) can be placed at the L_G pin. This capacitor value should be 300pF typical and 600pF max (see Table I). The slew rate will decrease with increasing C_{GL} (Fig.20). If further reduction of the slew rate is needed, a resistor (R_{DD}) can be placed in between the V_{DD} capacitor and the V_{DD} pin. This resistor value should be 0 Ω typical and 100 Ω max (see Table I).

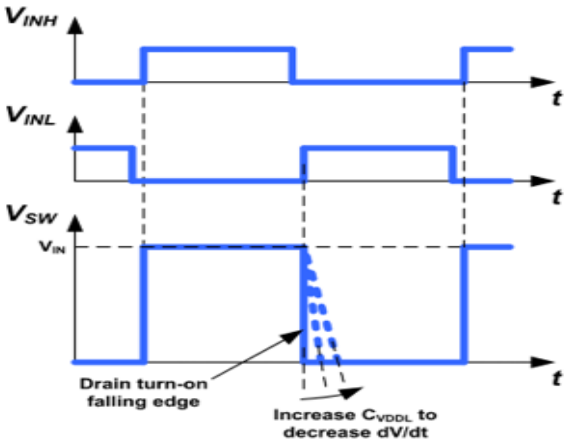


Fig.20. Turn-on dV/dt slew rate control

7.5. Connection Diagram

The following schematic (Fig.21) and table (Table II) show the typical connection diagram and recommended component values for the external filter capacitors and Zener diodes connected to the pins of the NV6252. These components should be placed as close as possible to the IC. Please see PCB Layout Guidelines for more information. For many applications, it is necessary to sense the cycle-by-cycle current flowing through the power FET. To sense the current flowing through the power IC, a standard current-sensing resistor can be placed in between the source and power ground (Fig.21). In this configuration, all of the surrounding components (C_{VCC}, C_{VDDL}, D_{ZL}, C_{GL} etc.) should be grounded with a single connection at the source.

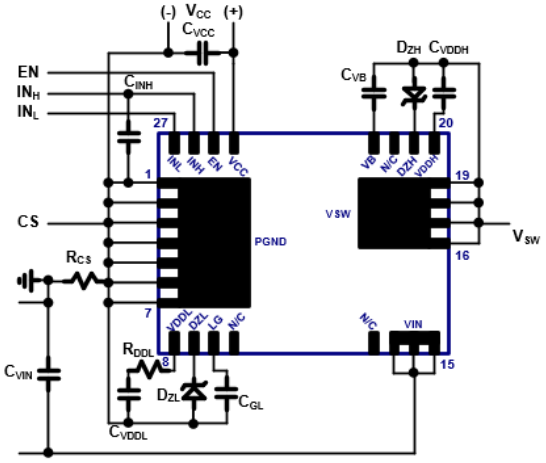


Fig.21. Typical connection diagram

7.6. Recommended Component Values

Table II provides the recommended component values for the external filter capacitors and resistors connected to the pins of the NV6252. These components should be placed as close as possible to the IC. Please see PCB Layout guidelines for more information. The Zener diode at the $DZ_{L,H}$ pins should be a low-current type with a flat Zener knee.

7.6.1. .Zener Selection

The Zener voltage is a critical parameter that sets the internal reference for gate drive voltage and another circuitry. The Zener diode needs to be selected such that the voltage on the $DZ_{L,H}$ pins are within their recommended operating conditions (5.8 V to 6.6 V) across operating temperature (-40°C to 125°C) and bias current (10 µA to 1 mA). To ensure effective operation, the current vs. voltage characteristics of the Zener diode should be measured down to 10µA to ensure flat characteristics across the current operating range (10 µA to 1 mA). Only the qualified Zener diodes as defined in Table III should be used. If the Zener selected by user does not ensure that the voltage on the $DZ_{L,H}$ pins are always within their recommended operating range, the functionality and reliability of the NV6252 can be impacted.

7.7. PCB Layout Guidelines

The design of the PCB layout is critical for good noise immunity, sufficient thermal management, and proper operation of the IC. A typical PCB layout example is shown on page 15.

The following rules should be followed carefully during the design of the PCB layout:

1) Place all IC filter and Programming components directly next to the IC. These components include (C_{VCC}, C_{VDDL}, R_{DDL}, DZ_L, C_{GL}, C_{VB}, C_{VDDH}, DZ_H).

2) Keep the ground trace of IC filter and programming components separate from P_{GND} trace. The ground trace of the IC filter and programming components should connect to the P_{GND} at a single point only. Do not run high P_{GND} currents through the low current ground trace of the filter components

3) For best thermal management, place thermal vias in the P_{GND} and V_{SW} pad areas to conduct the heat out through the bottom of the package and through the PCB board to other layers.

4) Use large PCB thermal planes (connected with thermal vias to the P_{GND} and V_{SW} pads) and additional PCB layers to reduce IC temperatures as much as possible .

5) For half-bridge layouts, do not extend copper planes from one IC across the components or pads of the other IC.

6) For multi-layer boards, do not place V_{SW} copper areas across P_{GND}-referenced components, and, do not place P_{GND} copper areas across V_{SW}-referenced copper areas. Keep them separate to avoid capacitive noise coupling between the low-side and high-side circuitry and to avoid possible faulty switching.

SYM	DESCRIPTION	PART NO.	SUPPLIER	MIN	TYP	MAX	UNITS
C_{GL}	C_{GL} gate capacitor				300	600	pF
R_{VDDL}	R_{VDDL} resistor				0	100	Ω

Table I. Low-side FET slew rate control recommended component values.

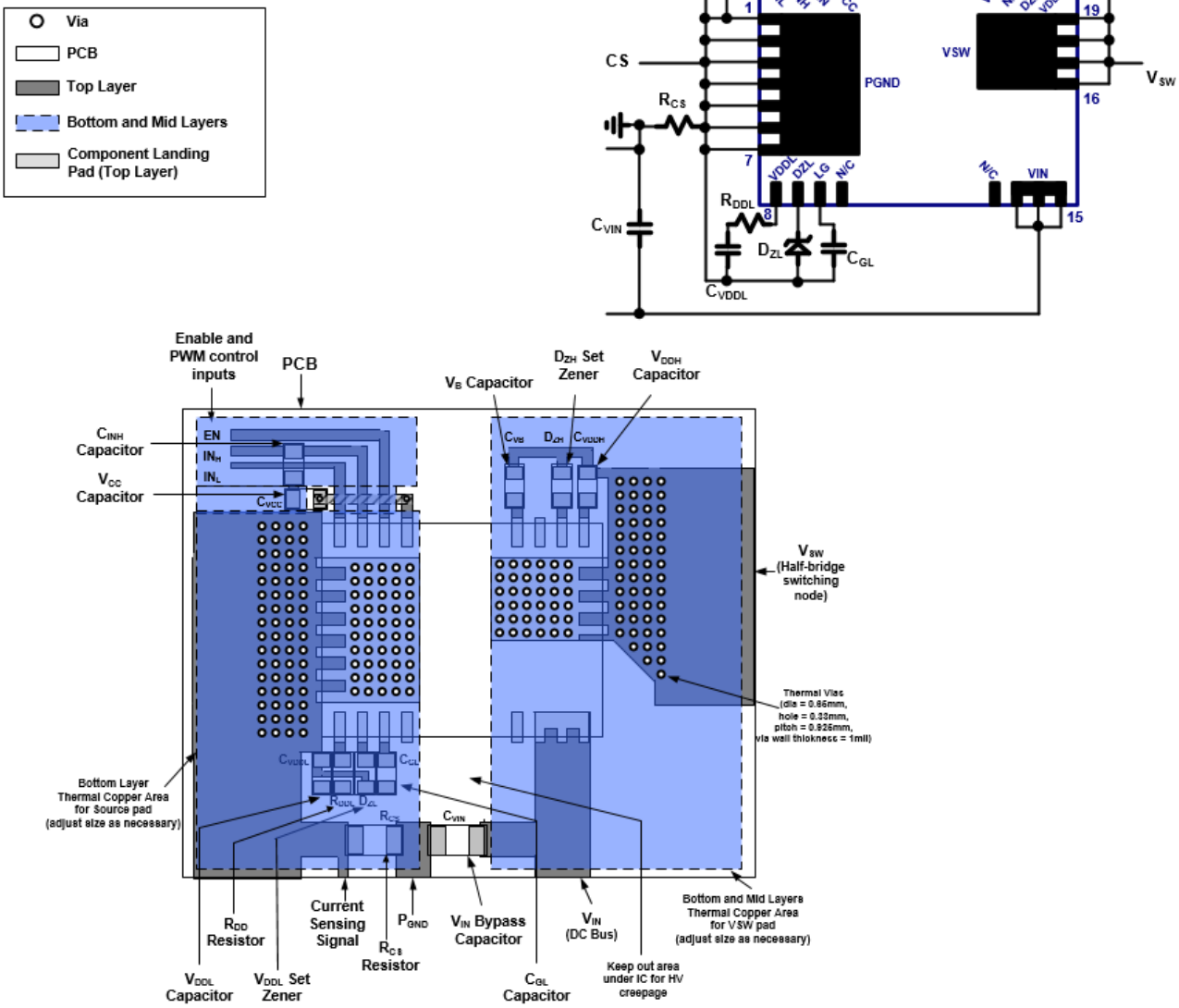
SYM	DESCRIPTION	PART NO.	SUPPLIER	MIN	TYP	MAX	UNITS
C_{VCC}	V_{CC} supply capacitor				0.1		µF
$C_{VDDL,H}$	V_{DDL} & V_{DDH} supply capacitor				0.01		µF
R_{DD}	Gate drive turn-on current set resistor				0		Ω
C_{GL}	C_{GL} gate capacitor				300		pF
R_{VDDL}	R_{VDDL} resistor				0	100	Ω
C_{INH}	IN_H pin capacitor				220		pF

Table II. Recommended component values.

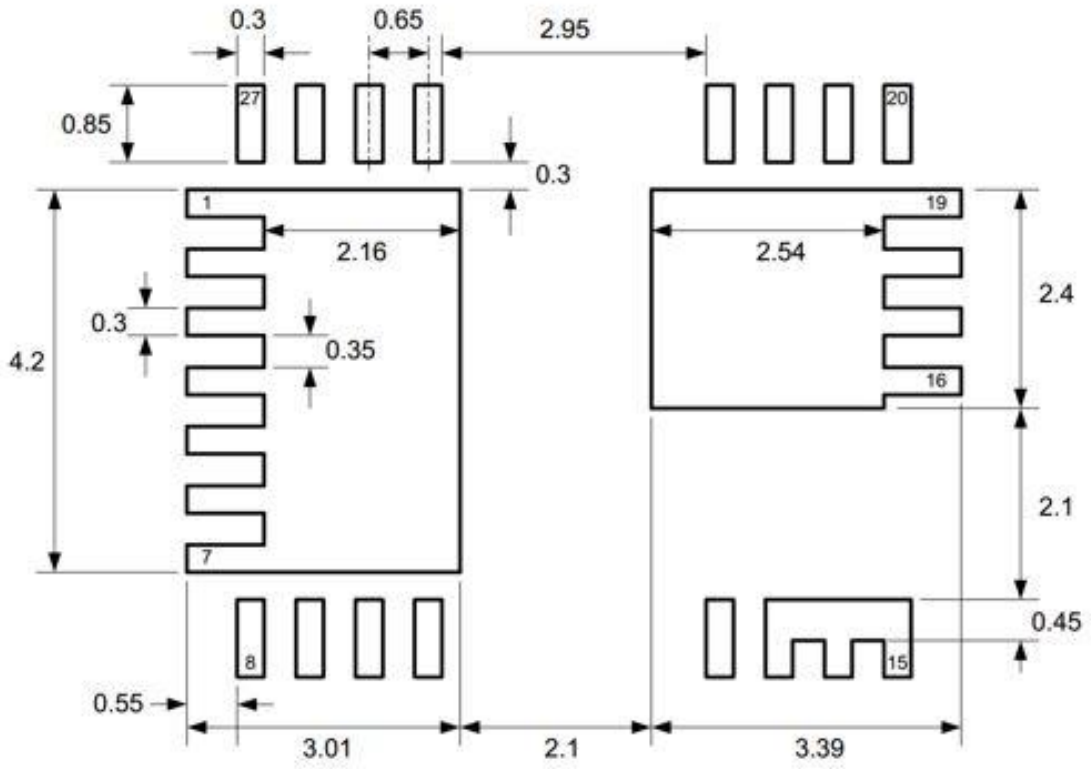
SYM	DESCRIPTION	PART NO.	SUPPLIER	MIN	TYP	MAX	UNITS
$DZ_{L,H}$	V_{DDL} and V_{DDH} set Zener diode (DZ_L and DZ_H pins)	BZT52B6V2 RHG	Taiwan Semiconductor Corporation		6.2		V
		MM3Z6V2ST1G	ON-Semiconductor		6.2		V
		PDZ6.2B.115	Nexperia (NXP)		6.2		V
		PLVA662A.215	Nexperia (NXP)		6.2		V
		LM3Z6V2T1	Leshan Radio Company		6.2		V

Table III. Qualified Zener diode parts to be used with NV6252.

8. PCB Layout Guidelines (2-layer board)



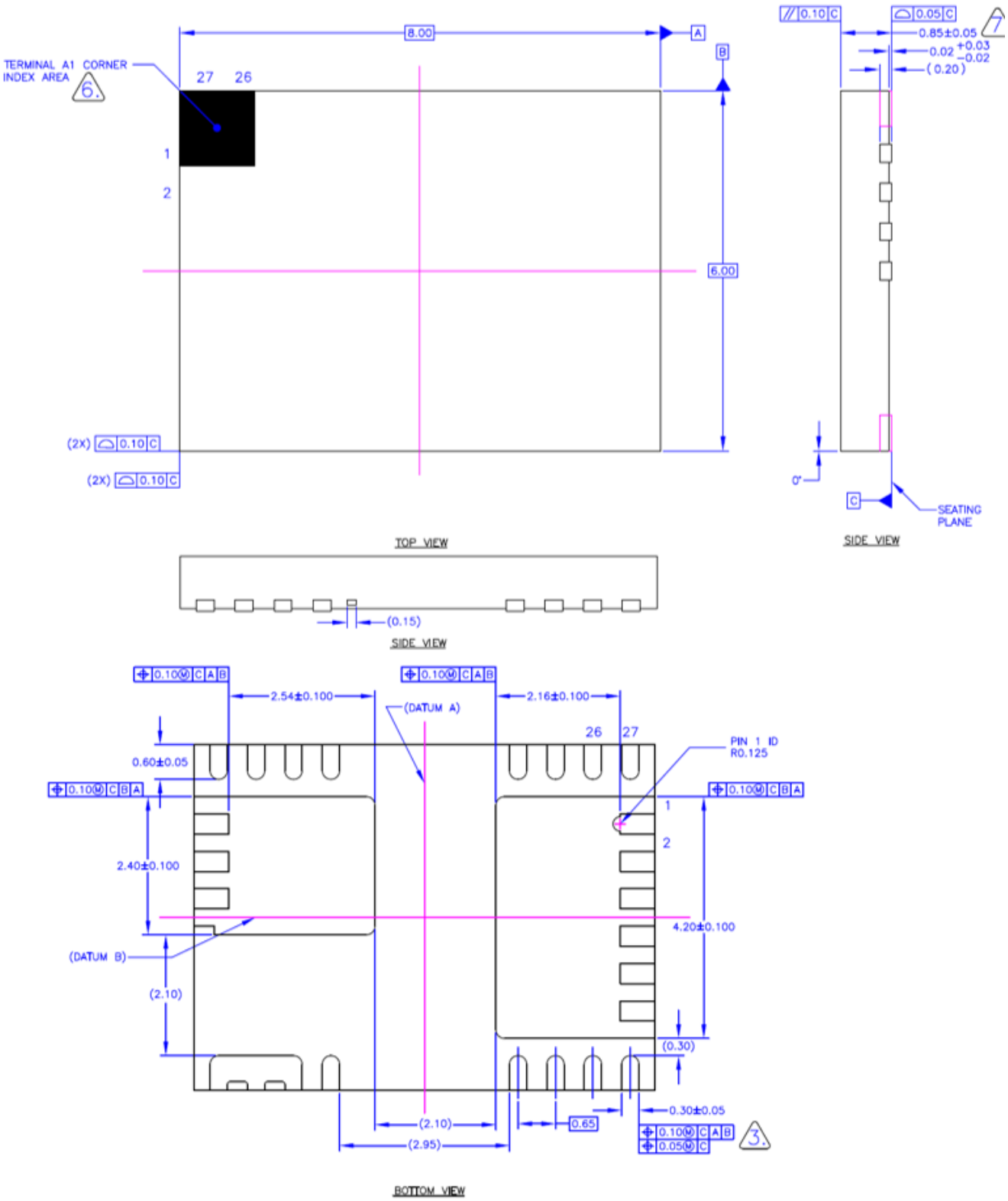
9. Recommended PCB Land Pattern



(Top View)

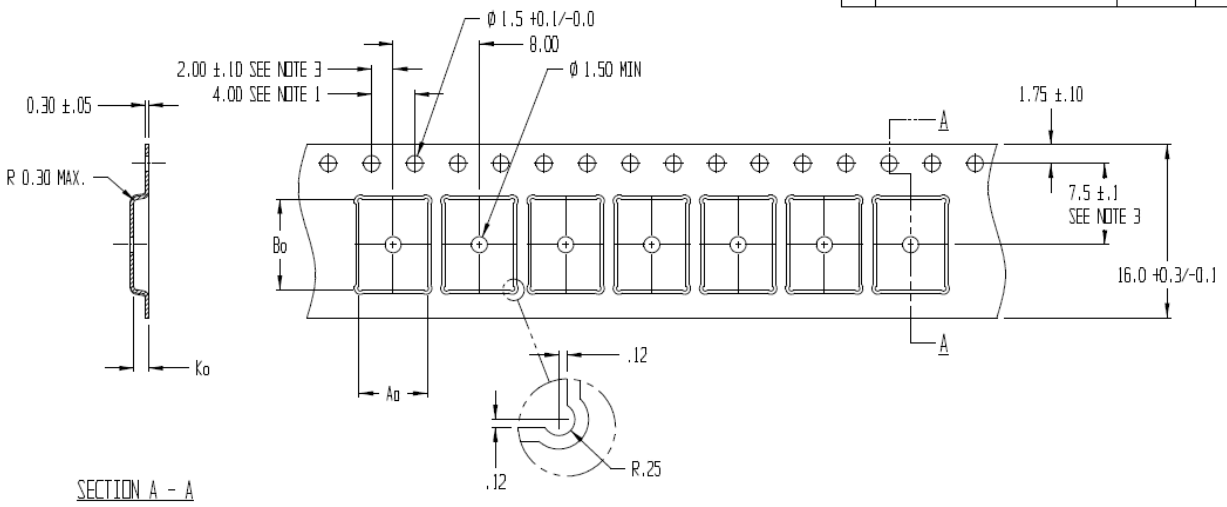
All dimensions are in mm

10. PQFN Package Outline



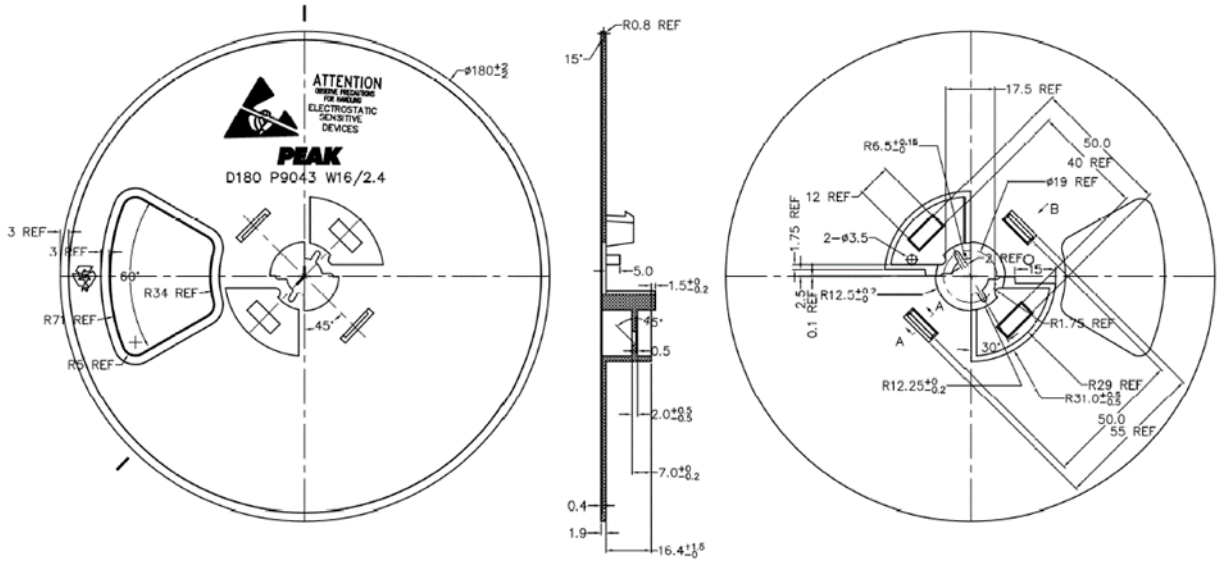
11. Tape and Reel Dimensions

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

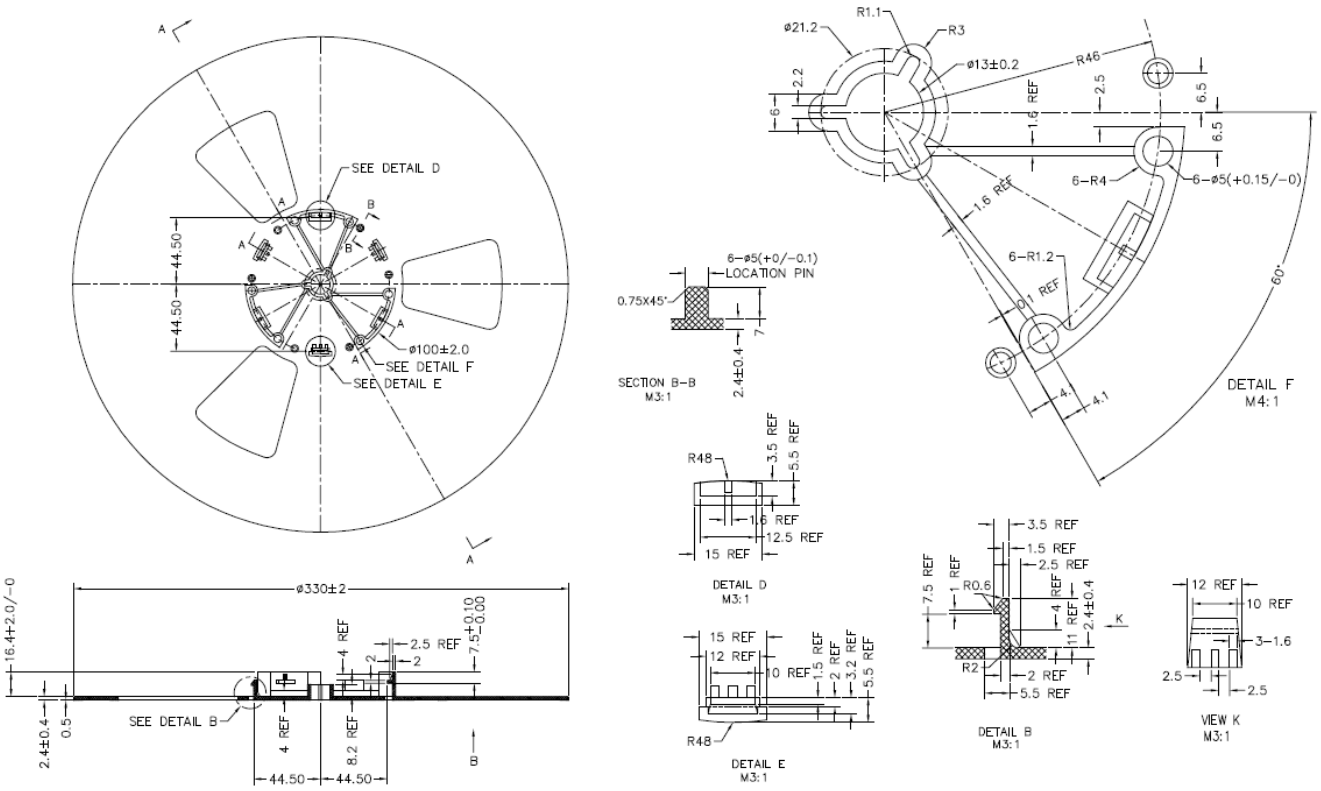


Ao = 6.35
Bo = 8.35
Ko = 1.40

7” Reel



13” Reel



12. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing (Tape & Reel)
NV6252	-40°C to +125°C T_{CASE}	-55°C to +150°C T_{CASE}	6 x 8 mm PQFN	3	1,000 : 7” Reel 5,000 : 13” Reel

Additional Information

Navitas Semiconductor Inc., 2101 E El Segundo Blvd, Suite 201, El Segundo, California 90245, USA. Contact info@navitassemi.com